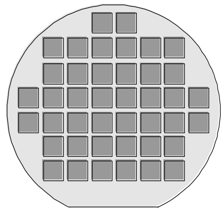
Chips or wafers

FEATURES

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage: 2.7V~5.5V
- LCD driving voltage: 8V~17V(V_{DD}-V_{EE})
- Interface

Driver		Controller
COMMON	SEGMENT	
An0107	An0108	MPU

- High voltage CMOS Process
- bare chip available

INTRODUCTION

The An0107 is a LCD driver LSI with 64 channel common outputs for dot matrix liquid crystal graphic display system. The device provides 64 bits shift register and 64 output drivers. It generates the timing signal to control the An0108.

The An0107 is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display in combination with the An0108 (64 channel segment driver).

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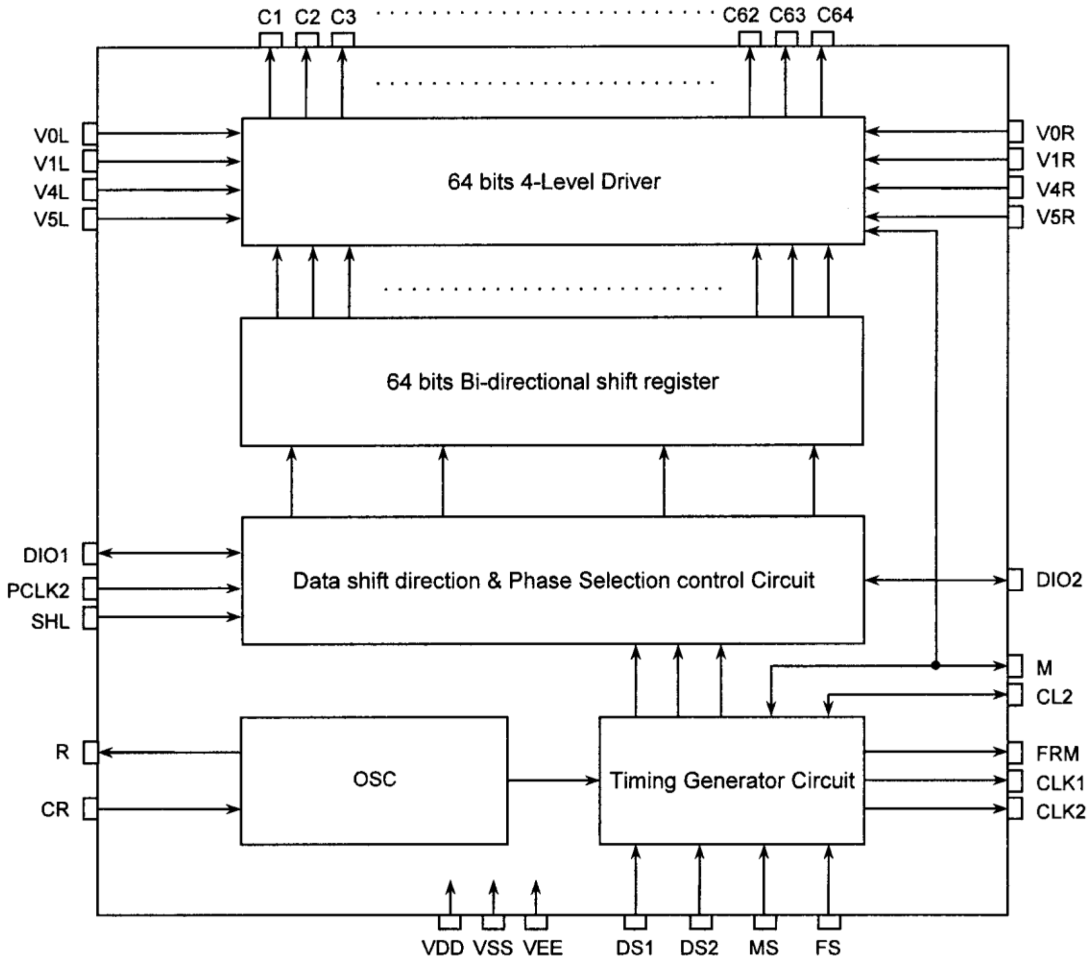
BLOCK DIAGRAM



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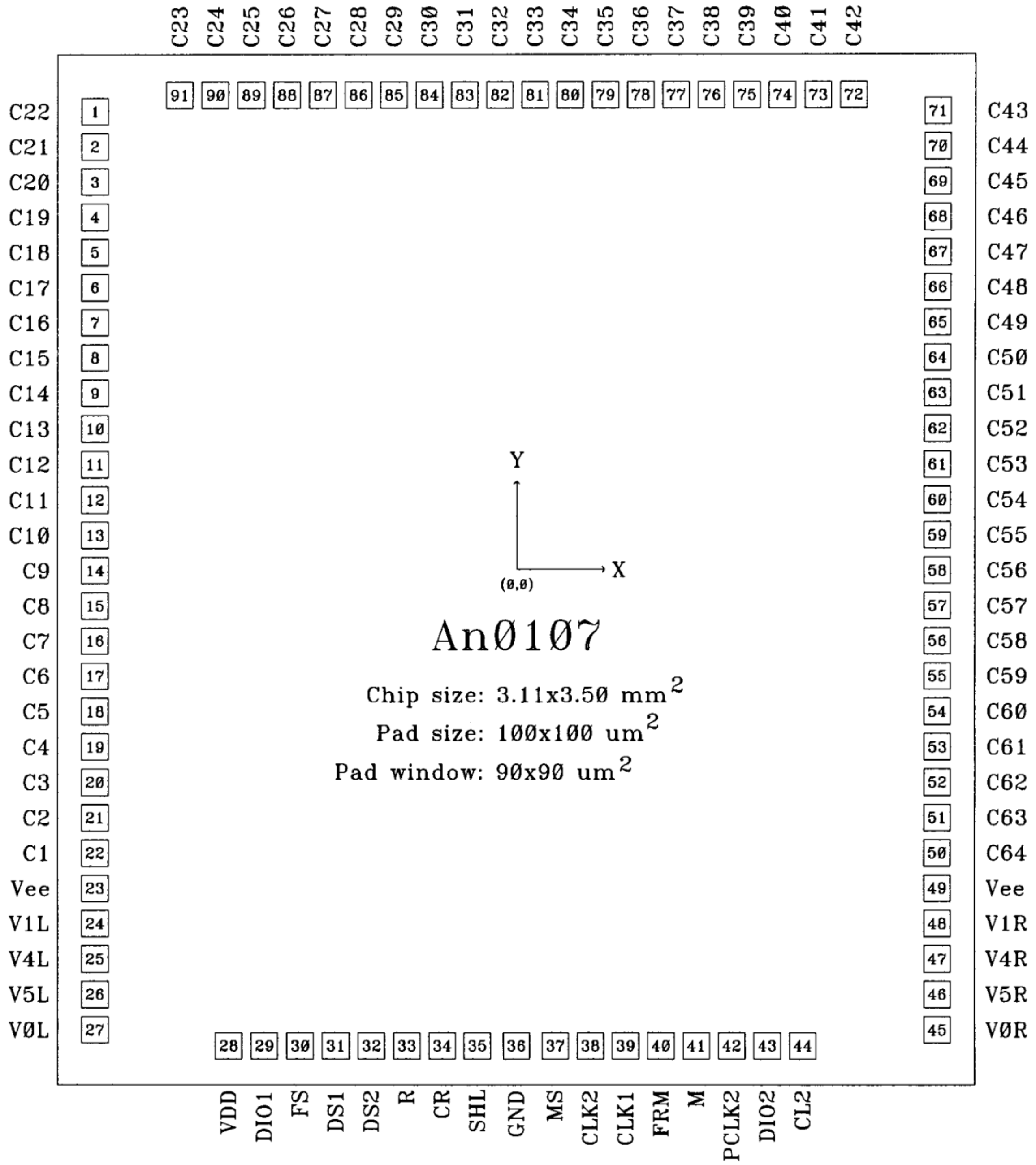
PAD DIAGRAM



Note: Connect substrate to VDD or floating.

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PAD LOCATION COORDINATES

Pad No	Pad Name	Coordinates		Pad No	Pad Name	Coordinates	
		X (µm)	Y (µm)			X (µm)	Y (µm)
1	C22	-1426.70	1556.10	47	V4R	1426.60	-1323.90
2	C21		1436.10	48	V1R		-1203.90
3	C20		1316.10	49	VEE		-1083.90
4	C19		1196.10	50	C64		-963.90
5	C18		1076.10	51	C63		-843.90
6	C17		956.10	52	C62		-723.90
7	C16		836.10	53	C61		-603.90
8	C15		716.10	54	C60		-483.90
9	C14		596.10	55	C59		-363.90
10	C13		476.10	56	C58		-243.90
11	C12		356.10	57	C57		-123.90
12	C11		236.10	58	C56		-3.90
13	C10		116.10	59	C55		116.10
14	C9		-3.90	60	C54		236.10
15	C8		-123.90	61	C53		356.10
16	C7		-243.90	62	C52		476.10
17	C6		-363.90	63	C51		596.10
18	C5		-483.90	64	C50		716.10
19	C4		-603.90	65	C49		836.10
20	C3		-723.90	66	C48		956.10
21	C2		-843.90	67	C47		1076.10
22	C1		-963.90	68	C46		1196.10
23	VEE		-1083.90	69	C45		1316.10
24	V1L		-1203.90	70	C44		1436.10
25	V4L		-1323.90	71	C43		1556.10
26	V5L		-1443.90	72	C42	1140.00	1611.80
27	V0L		-1563.90	73	C41	1020.00	
28	VDD	-974.90	-1618.10	74	C40	900.00	
29	DIO1	-854.90		75	C39	780.00	
30	FS	-734.90		76	C38	660.00	
31	DS1	-614.90		77	C37	540.00	
32	DS2	-494.90		78	C36	420.00	
33	R	-374.90		79	C35	300.00	
34	CR	-254.90		80	C34	180.00	
35	SHL	-134.90		81	C33	60.00	
36	GND	-1.90		82	C32	-60.00	
37	MS	131.10		83	C31	-180.00	
38	CLK2	251.10		84	C30	-300.00	
39	CLK1	371.10		85	C29	-420.00	
40	FRM	491.10		86	C28	-540.00	
41	M	611.10		87	C27	-660.00	
42	PCLK2	731.10		88	C26	-780.00	
43	DIO2	851.10		89	C25	-900.00	
44	CL2	971.10		90	C24	-1020.00	
45	VOR	1426.60	-1563.90	91	C23	-1140.00	
46	V5R	1426.60	-1443.90				

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PIN DESCRIPTION

<table>
<tr><th>Pin Number
QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>28</td><td>VDD</td><td rowspan="3">Power</td><td>For internal logic circuit (+2.7~+5.5V)</td></tr>
<tr><td>36</td><td>VSS</td><td>GND (0V)</td></tr>
<tr><td>23, 49</td><td>VEE</td><td>For LCD driver circuit</td></tr>
<tr><td>27, 45</td><td>V0L, V0R</td><td rowspan="4">Power</td><td rowspan="4">Bias supply voltage terminals to drive LCD.<table><tr><th>Select Level</th><th>Non-Select Level</th></tr><tr><td>V0L (R), V5L (R)</td><td>V1L (R), V4L (R)</td></tr></table>The same voltage should connect V0L and V0R (V1L & V1R, V4L & V4R, V5L & V5R).</td></tr>
<tr><td>24, 48</td><td>V1L, V1R</td></tr>
<tr><td>25, 47</td><td>V4L, V4R</td></tr>
<tr><td>26, 46</td><td>V5L, V5R</td></tr>
<tr><td>37</td><td>MS</td><td>Input</td><td>Selection of master/slave mode
i) Master mode (MS=1):
DIO1, DIO2, CL2 and M are output state.
ii) Slave mode (MS=0):
SHL=1: DIO1 is input state (DIO2 is output state)
SHL=0: DIO2 is input state (DIO1 is output state)
CL2 and M are input state.</td></tr>
<tr><td>35</td><td>SHL</td><td>Input</td><td>Selection of data shift direction.<table><tr><th>SHL</th><th>Data Shift Direction</th></tr><tr><td>H</td><td>DIO1→C1 ... C64→DIO2</td></tr><tr><td>L</td><td>DIO2→C64 ... C1→DIO1</td></tr></table></td></tr>
<tr><td>42</td><td>PCLK2</td><td>Input</td><td>Selection of shift clock (CL2) phase.<table><tr><th>PCLK2</th><th>Data Clock (CL2) Phase</th></tr><tr><td>H</td><td>Data shift at the rising edge of CL2</td></tr><tr><td>L</td><td>Data shift at the falling edge of CL2</td></tr></table></td></tr>
<tr><td>30</td><td>FS</td><td>Input</td><td>Selection of oscillation frequency.
i) Master mode:
When the frame frequency is 70Hz, the oscillation frequency should be
fosc=430kHz at FS=1 (VDD)
fosc=215kHz at FS=0 (VSS)
ii) Slave mode:
Connect to VDD.</td></tr>
<tr><td>31
32</td><td>DS1
DS2</td><td>Input</td><td>Selection of display duty.
i) Master mode:<table><tr><th>DS1</th><th>DS2</th><th>Duty</th></tr><tr><td rowspan="2">L</td><td>L</td><td>1/48</td></tr><tr><td>H</td><td>1/64</td></tr><tr><td rowspan="2">H</td><td>L</td><td>1/96</td></tr><tr><td>H</td><td>1/128</td></tr></table>ii) Slave mode:
Connect to VDD.</td></tr>
</table>

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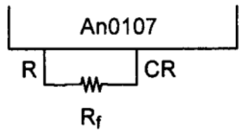
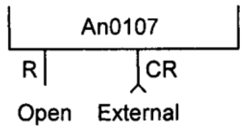
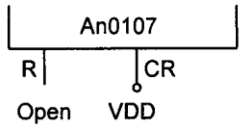
<table>
<tr><th>Pin Number
QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>33
34</td><td>R
CR</td><td></td><td>RC Oscillator (Built-in capacitor)
i) Master mode: Use these terminals as shown below.

ii) Slave mode: Stop the oscillator as shown below.
</td></tr>
<tr><td>39
38</td><td>CLK1
CLK2</td><td>Output</td><td>Operating clock output for the An0108
i) Master mode: connection to CLK1 and CLK2 of the An0108
ii) Slave mode: open</td></tr>
<tr><td>40</td><td>FRM</td><td>Output</td><td>Synchronous frame signal.
i) Master mode: connection to FRM of the An0108
ii) Slave mode: open</td></tr>
<tr><td>41</td><td>M</td><td>Input/
Output</td><td>Alternating signal input for LCD driving.
i) Master mode: output state
Connection to M of the An0108
ii) Slave mode: input state
Connection to the controller</td></tr>
<tr><td>44</td><td>CL2</td><td>Input/
Output</td><td>Data shift clock
i) Master mode: output state
Connection to CL of the An0108
ii) Slave mode: input state
Connection to shift clock terminal of the controller.</td></tr>
<tr><td>29
43</td><td>DIO1
DOI2</td><td>Output</td><td>Data input/output pin of internal shift register.
<table>
<tr><th>MS</th><th>SHL</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>22-1
91-50</td><td>C1-C64</td><td>Output</td><td>Common signal output for LCD driving.
<table>
<tr><th>Data</th><th>M</th><th>out</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td>V1</td></tr>
<tr><td>H</td><td>V4</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>V5</td></tr>
<tr><td>H</td><td>V0</td></tr>
</table></td></tr>
</table>

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ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Operating Voltage	V_{DD}	-0.3 ~ +7.0	V	(1)
Supply Voltage	V_{EE}	V_{DD}-19.0 ~ V_{DD}+0.3	V	(4)
Driver Supply Voltage	V_B	-0.3 ~ V_{DD}+0.3	V	(1), (2)
	V_{LCD}	V_{EE} -0.3 ~ V_{DD}+0.3	V	(3), (4)
Operating Temperature	T_{OPR}	-30 ~ +85	°C	-
Storage Temperature	T_{STG}	-55 ~ +125	°C	-

Notes:

1. Based on V_{SS}=0V.
2. Applies to input terminals and I/O terminals at high impedance. (Except V0L(R), V1L(R), V4L(R) and V5L(R)).
3. Applies to V0L(R), V1L(R), V4L(R) and V5L(R).
4. Voltage level: $V_{DD} \geq$ V0L=V0R $\geq$ V1L=V1R $\geq$ V4L=V4R $\geq$ V5L=V5R $\geq V_{EE}$.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD} =+5.0V, V_{SS}=0V, |V_{DD}- V_{EE}|=8~17V, TA= -30~+85°C)

Characteristic	Symbol	Test condition	Min	Typ	Max	Unit	Note
Operating Voltage	V_{DD}	-	2.7	-	5.5	V	
Input High Voltage	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V	(1)
Input Low Voltage	V_{IL}	-	V_{SS}	-	0.3V_{DD}	V	
Output High Voltage	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	-	V	(2)
Output Low Voltage	V_{OL}	I_{OL}=+0.4mA	-	-	0.4	V	
Input Leakage Current	I_{LKG}	V_{IN} =V_{DD}-V_{SS}	-1.0	-	1.0	μA	(1)
OSC Frequency	f_{OSC}	Rf=47KΩ±2%	315	450	585	kHz	
On resistance (V_{DIV}-C_i)	R_{ON}	V_{DD}-V_{EE}=17V Load current = ±150μA	-	-	1.5	KΩ	
Operating Current	I_{DD1}	Master mode; 1/128 duty	-	-	180	μA	(3)
	I_{DD2}	Slave mode; 1/128 duty	-	-	30	μA	(4)
Supply Current	I_{EE}	Master mode; 1/128 duty	-	-	20	μA	(5)
Operating Frequency	f_{OP1}	Master mode; External clock	50	-	600	kHz	
	f_{OP2}	Slave mode	0.5	-	1500	kHz	

Notes:

1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the output state.
3. This value is specified at about current flowing through V_{SS}. Internal oscillation circuit: Rf=47kΩ. Each terminals of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
4. This value is specified at about current flowing through V_{SS}. Each terminals is DS1, DS2, FS, SHL, PCLK2 and CR is connected to VDD, MS is connected to V_{SS}. CL2, M, DIO1 is external clock.
5. This value is specified at the current flowing through V_{EE}. Don't connect to V_{LCD} (V1~V5).

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AC CHARACTERISTICS (V_{DD} =5V±10%, Ta=-30~+85°C)

Master Mode (MS=V_{DD}, PCLK2=V_{DD})

Characteristic	Symbol	Min	Typ	Max	Unit
Data Setup Time	t_{SU}	20	-	-	µs
Data Hold Time	t_{DH}	40	-	-	µs
Data Delay Time	t_D	5	-	-	µs
FRM Delay Time	t_{DF}	-2	-	2	µs
M Delay Time	t_{DM}	-2	-	2	µs
CL2 Low Level Width	t_{WLC}	35	-	-	µs
CL2 High Level Width	t_{WHC}	35	-	-	µs
CLK1 Low Level Width	t_{WL1}	700	-	-	ns
CLK2 Low Level Width	t_{WL2}	700	-	-	ns
CLK1 High Level Width	t_{WH1}	2100	-	-	ns
CLK2 High Level Width	t_{WH2}	2100	-	-	ns
CLK1-CLK2 Phase Difference	t_{D12}	700	-	-	ns
CLK2-CLK1 Phase Difference	t_{D21}	700	-	-	ns
CLK1, CLK2 Rise/Fall Time	t_R/t_F	-	-	150	ns

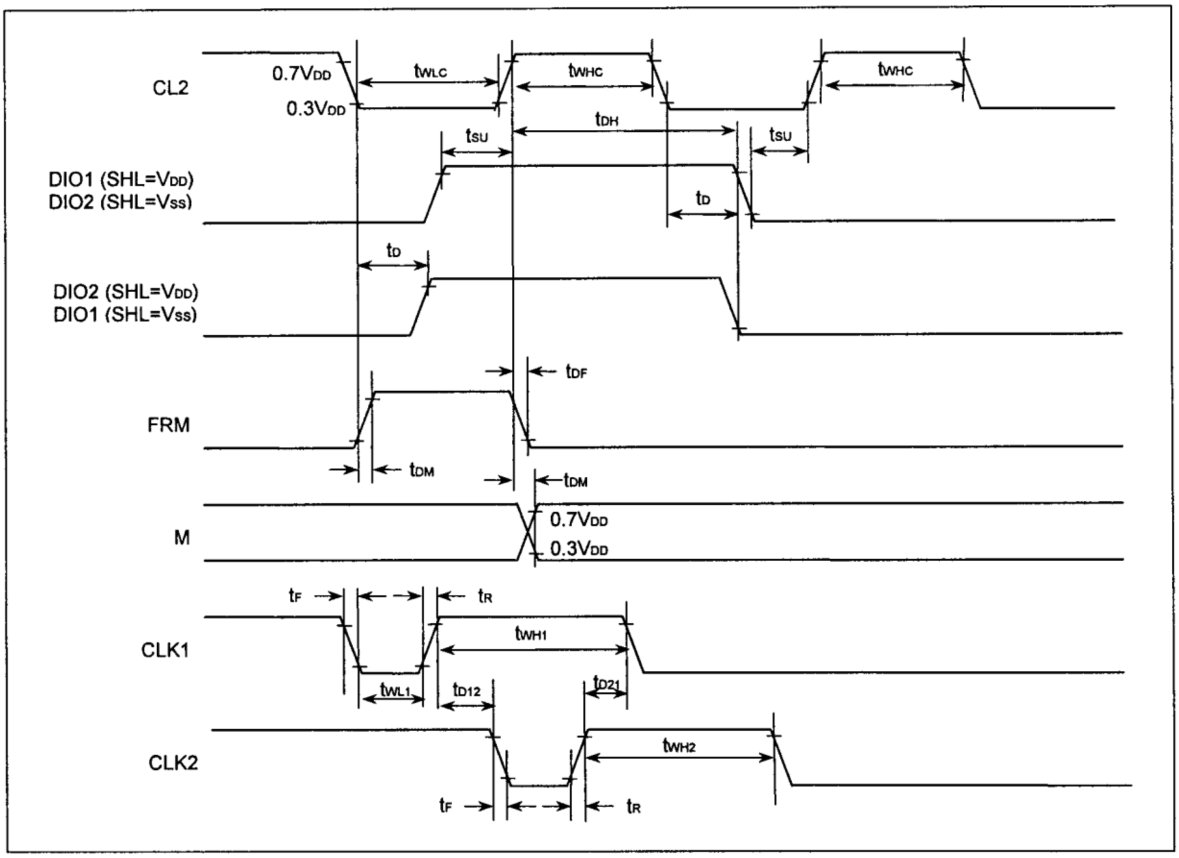

Figure 1. AC characteristics (Master Mode)

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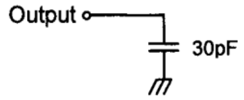
Slave Mode (MS=V_{SS})

Characteristic	Symbol	Min	Typ	Max	Unit	Note
CL2 Low Level Width	t_{WLC1}	450	-	-	ns	PCLK2=V_{SS}
CL2 High Level Width	t_{WHC1}	150	-	-	ns	PCLK2=V_{SS}
CL2 Low Level Width	t_{WLC2}	150	-	-	ns	PCLK2=V_{DD}
CL2 High Level Width	t_{WHC2}	450	-	-	ns	PCLK2=V_{DD}
Data Setup Time	t_{SU}	100	-	-	ns	
Data Hold Time	t_{DH}	100	-	-	ns	
Data Delay Time	t_D	-	-	200	ns	(Note)
Output Data Hold Time	t_H	10	-	-	ns	
CL2 Rise/Fall Time	t_R/t_F	-	-	30	ns	

Note: Connect load CL = 30pF



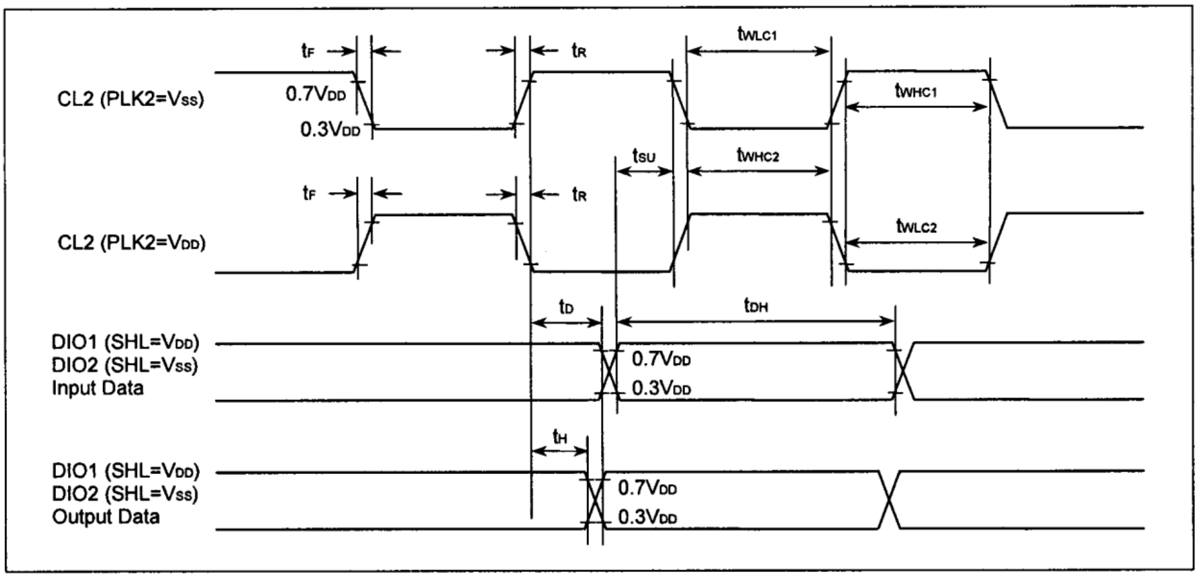


Figure 2. AC characteristics (Slave Mode)

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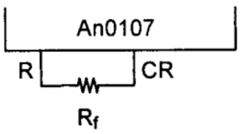
FUNCTION DESCRIPTION

1. RC Oscillator

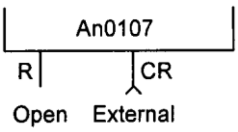
The RC Oscillator generates CL2, M, FRM, of the An0107, and CLK1, CLK2 of the An0108 by the oscillation resister R and internal capacitor C. When selecting the master/slave mode, the oscillation circuit is as following:

i) **Master Mode**: In the master mode, use these terminals as shown below.

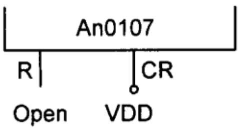
For Internal Oscillation (Rf=47kΩ)



For External Clock



ii) **Slave Mode**: In the slave mode, stop the oscillator as shown below.



2. Timing Generation Circuit

It generates CL2, M, FRM, CLK1, and CLK2 by the frequency from oscillation circuit.

1) Selection of Master/Slave (MS) Mode

When MS is H, it generates CL2, M, FRM, CLK1, and CLK2 internally.

When MS is L, it operates by receiving M and CL2 from the master device.

2) Frequency Selection (FS)

To adjust FRM by 70Hz, the oscillation frequency should be as following:

FS	Oscillation Frequency
H	f_{OSC} = 430kHz
L	f_{OSC} = 215kHz

In the slave mode, it is connected to V_{DD}.

3) Duty Selection (DS1, DS2)

It provides various duty selection according to DS1, DS2.

DS1	DS2	Duty
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

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3. Data Shift & Phase Select Control

1) Phase Selection

It is a circuit to shift data on synchronization of rising edge or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shifts on rising edge of CL2
L	Data shifts on falling edge of CL2

2) Data Shift Direction Selection

When MS is connected to V_{DD}, DIO1 and DIO2 terminal is only output.

When MS is connected to V_{SS}, it depends on the SHL.

MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1 → C64
	L	Output	Output	C64 → C1
L	H	Input	Output	DIO1 → C1 ... C64 → DIO2
	L	Output	Input	DIO2 → C64 ... C1 → DIO1

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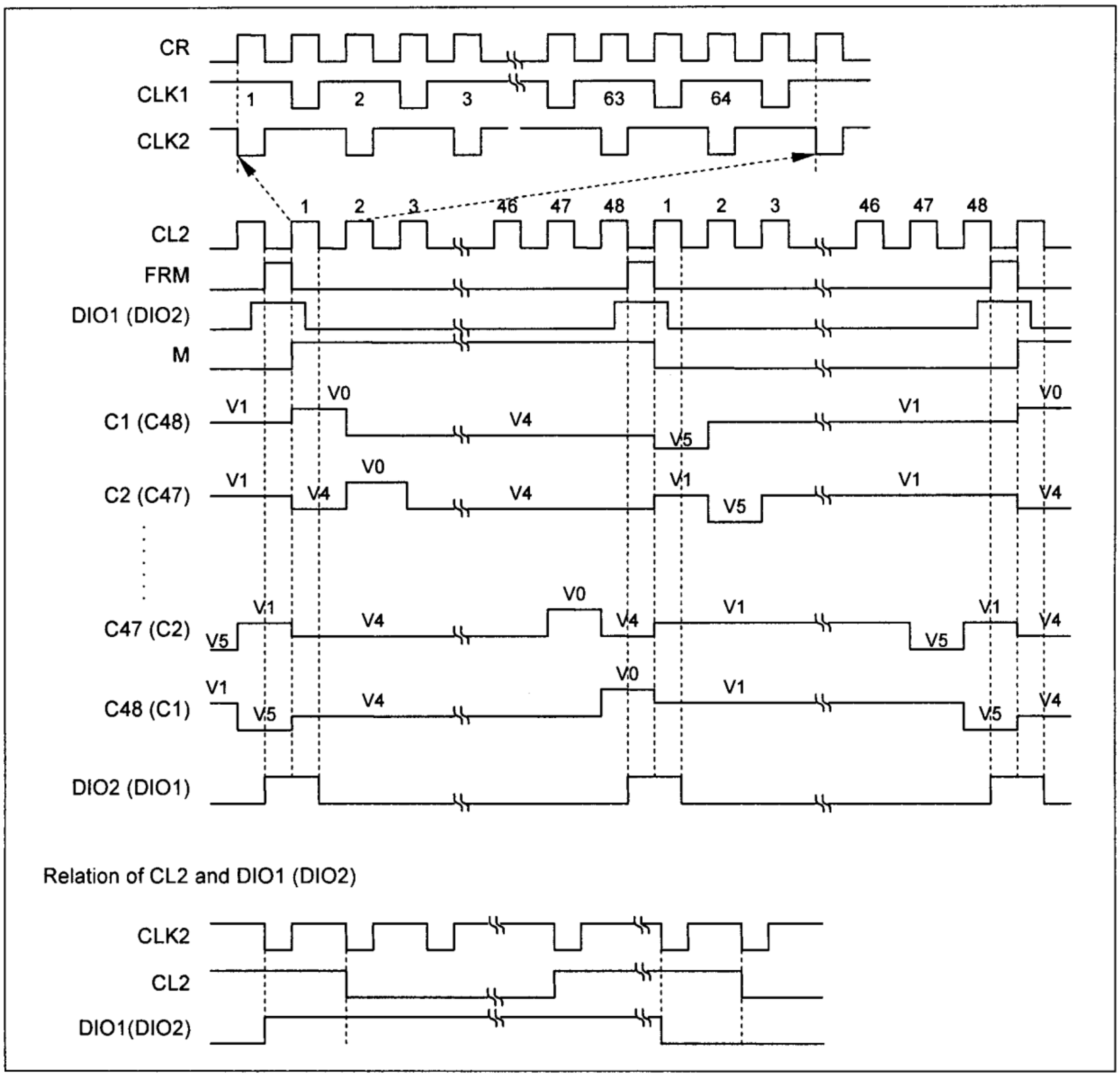
TIMING DIAGRAM

1. 1/48 Duty Timing (Master Mode)

Condition: DS1=L, DS2=L, SHL=H(L), PCLK2=H



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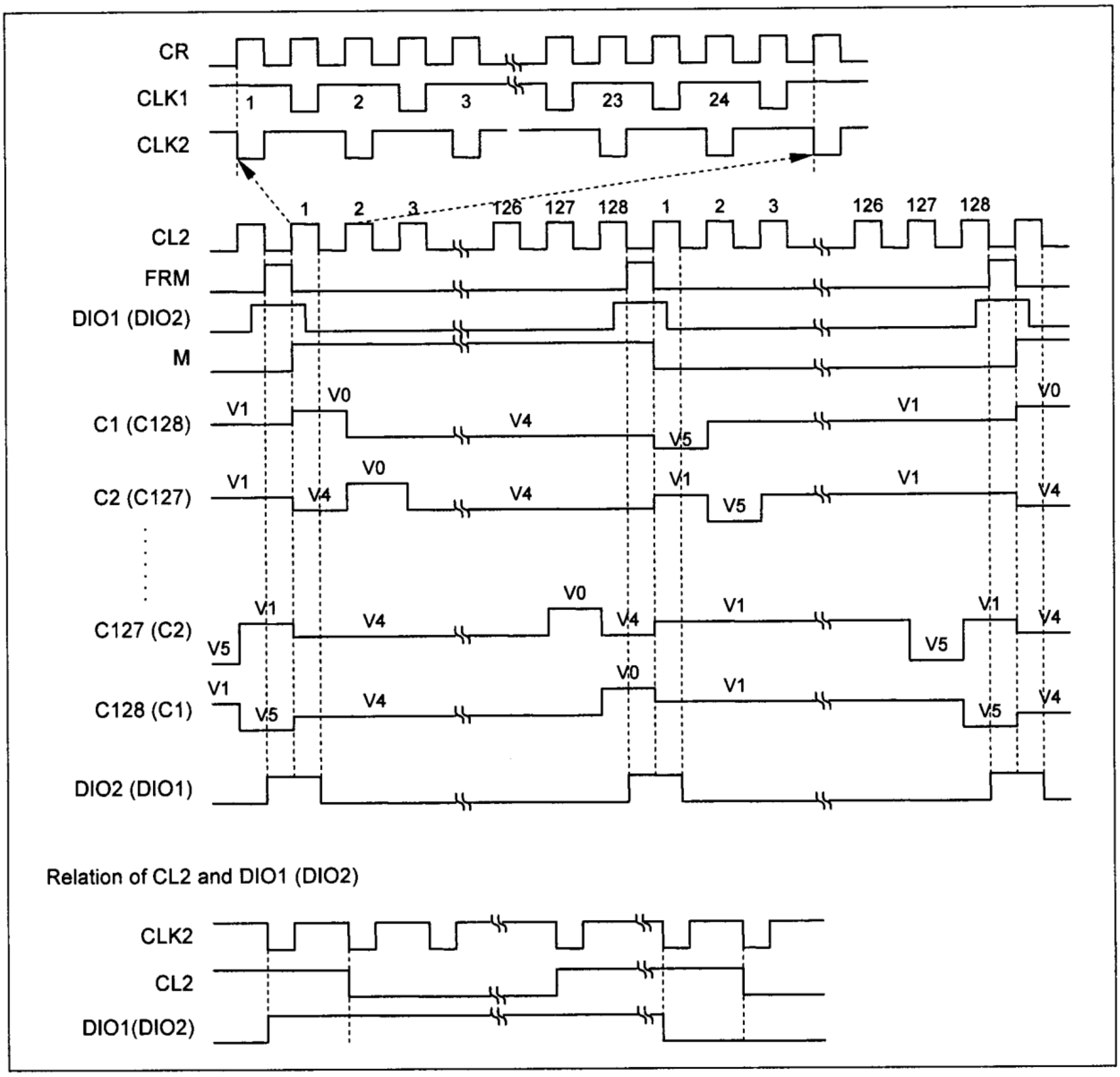
2. 1/128 Duty Timing (Master Mode)

Condition: DS1=H, DS2=H, SHL=H(L), PCLK2=H



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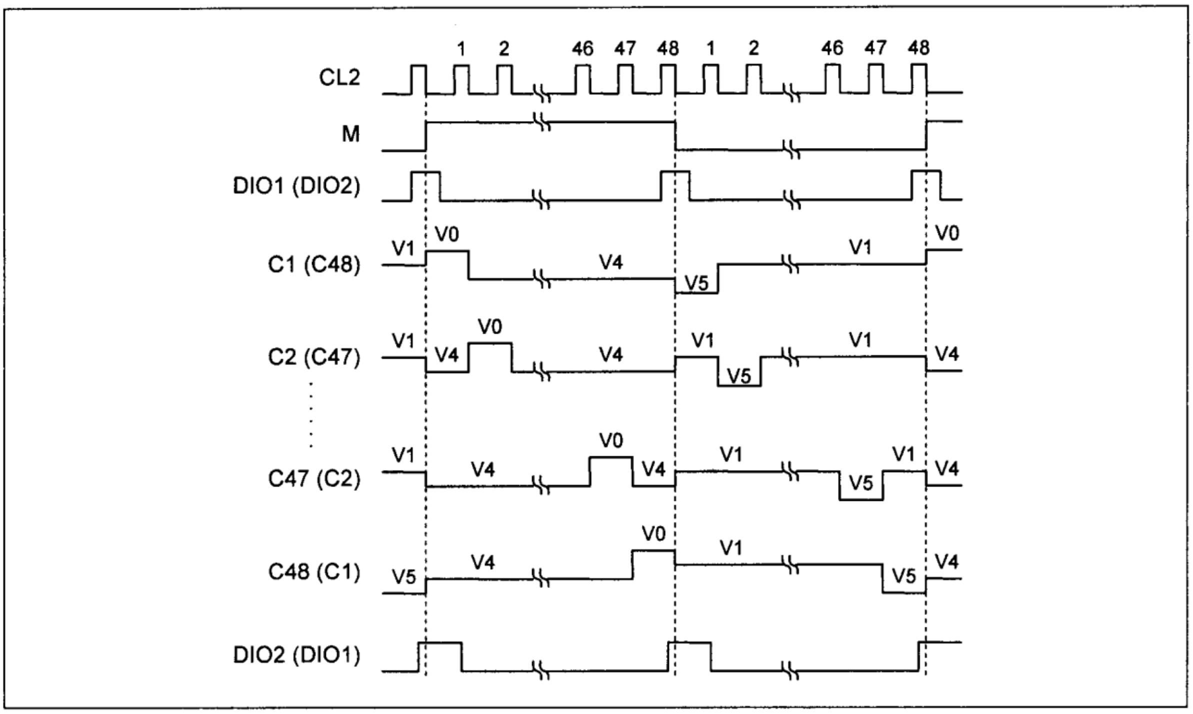
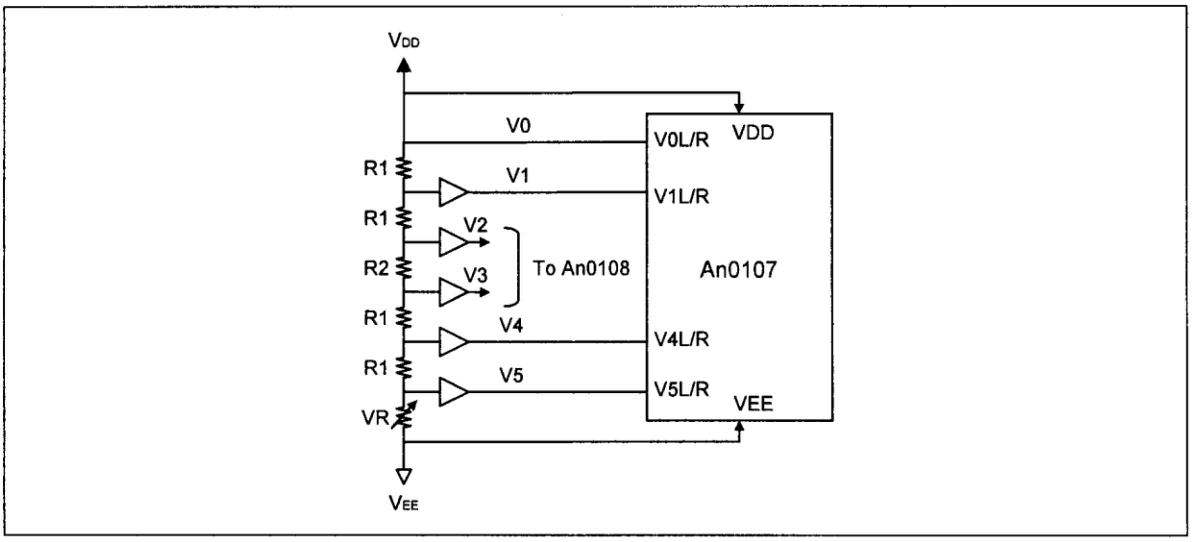
3. 1/48 Duty Timing (Slave Mode)

Condition: SHL=H(L), PCLK2=L



4. Power Driver Circuit



Relation of Duty & Bias

Duty	Bias	RDIV
1/48	1/8	R2 = 4R1
1/64	1/9	R2 = 5R1
1/96	1/11	R2 = 7R1
1/128	1/12	R2 = 8R1

When duty factor is 1/48, the value of R1 & R2 should satisfy

R1/(4R1+R2)=1/8
R1=3KΩ, R2=12KΩ

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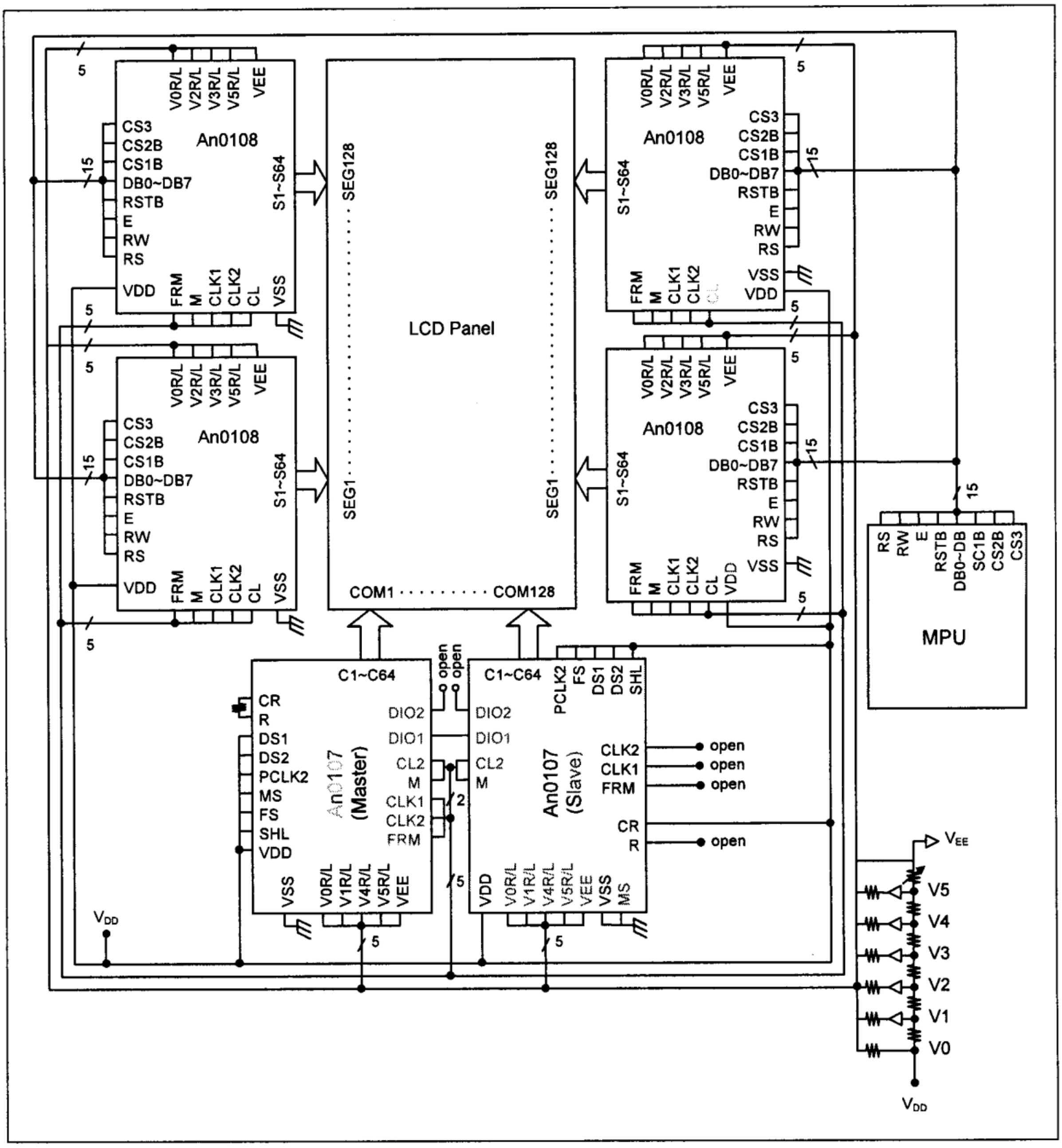
APPLICATION CIRCUIT

1/128 duty Segment driver (An0108) Interface circuit



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