An1990 SPECIFICATION

FEATURES:

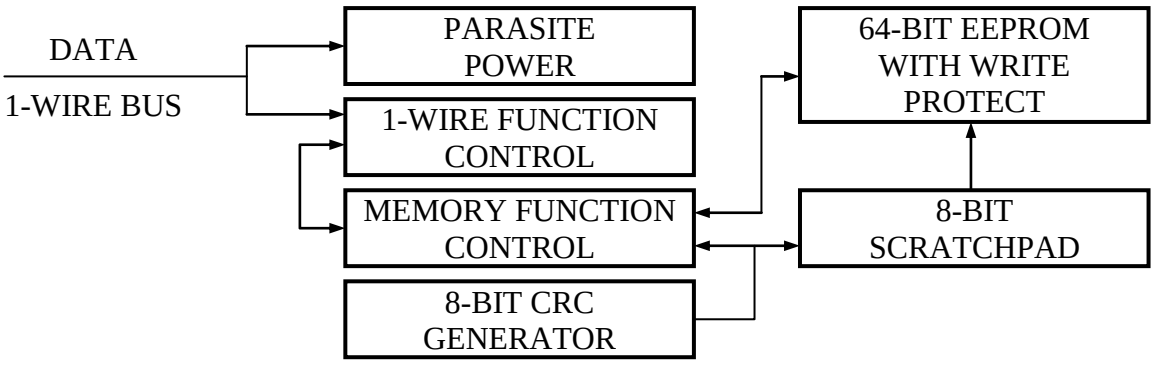
- 64-bits EEPROM communicates with the economy of one signal plus ground;
- Unique, one-time write protection 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures traceability;
- Built-in multidrop controller ensures compatibility with other MicroLAN™ products;
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits per second;
- Write voltage range of 4.0V to 4.5V from -10°C to +70°C;
- Read voltage range of 2.5V to 5.3V from -10°C to +70°C;
- Burn voltage 11.0V from -10°C to + 70°C.

TRANSACTION SEQUENCE

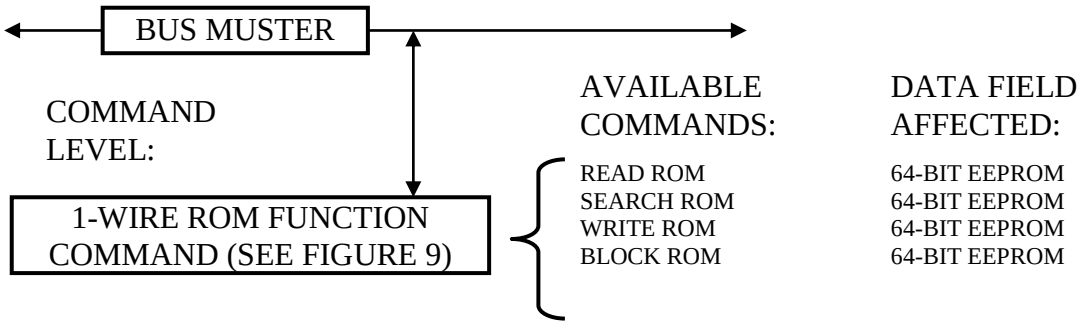
The protocol for accessing the An1990 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command

BLOCK DIAGRAM (Figure 1)



HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL (Figure 2)



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MEMORY STRUCTURE (Figure 3)

EEPROM: 8 BYTE OF 8 BIT)

ADDRESS:	0007h	0006h	0005h	0004h	0003h	0002h	0001h	0000h
	7	6	5	4	3	2	1	0
	MSB							LSB

BYTE0 FAMILY CODE
BYTE 6 SERIAL NUMBER
……
BYTE 6 SERIAL NUMBER
BYTE7 CRC CODE

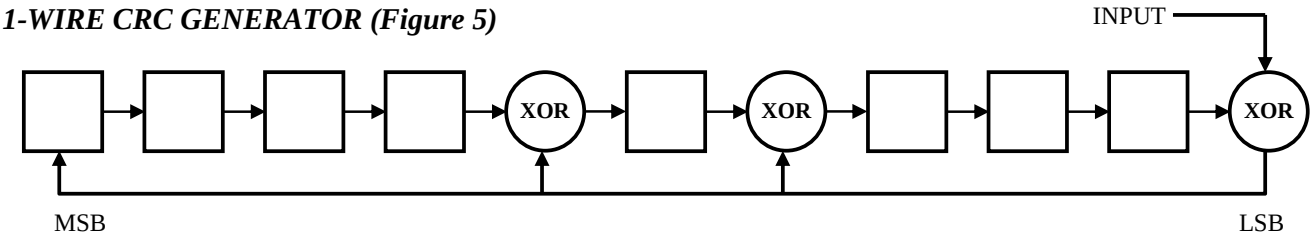
64-BIT ONE-TIME WRITE PROTECTION EEPROM

Each AN1990 contains a unique EEPROM code that is 64 bits long. The first eight bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits (See Figure 4). The 64-bit one-time write protection EEPROM and ROM Function Control section allow the AN1990 to operate as a 1-Wire device and follow the 1-Wire protocol detailed in the section "1-Wire Bus System". The memory functions required to read and program the EEPROM sections of the AN1990 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM functions flow chart (Figure 9). The 1-Wire bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Search ROM. The 1-Wire CRC of the ROM is generated using the polynomial X8 + X5 + X4 + 1. Figure 5 shows a hardware implementation of this CRC generator. The shift register acting as the CRC accumulator is initialised to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the eighth bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeroes. There are additional two ROM function commands: 3) Write ROM - writing unique number, 4) Block ROM - protection unique number from changing.

ONE-TIME WRITE PROTECTION EEPROM (Figure 4)

8-BIT CRC CODE		48-BIT SERIAL NUMBER		8-BIT FAMILY CODE	
MSB	LSB	MSB	LSB	MSB	LSB

1-WIRE CRC GENERATOR (Figure 5)



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INITIALIZATION

All transactions on the 1-Wire bus begin with an initialisation sequence. The initialisation sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the AN1990 is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 6):

Read ROM [33H]

This command allows the bus master to read the AN1990's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can be used only if there is a single AN1990 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired- AND result).

Search ROM [FOH]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

Write ROM [3CH]

Command allows to write a unique 64-bit number. The command can be executed only with not more than one AN1990 IC connected to the bus, otherwise a failure can occur.

Block ROM [35H]

The command ensures one-time write protection of the unique 64-bit number. After the Block ROM command execution it is not possible to execute a Write ROM command.

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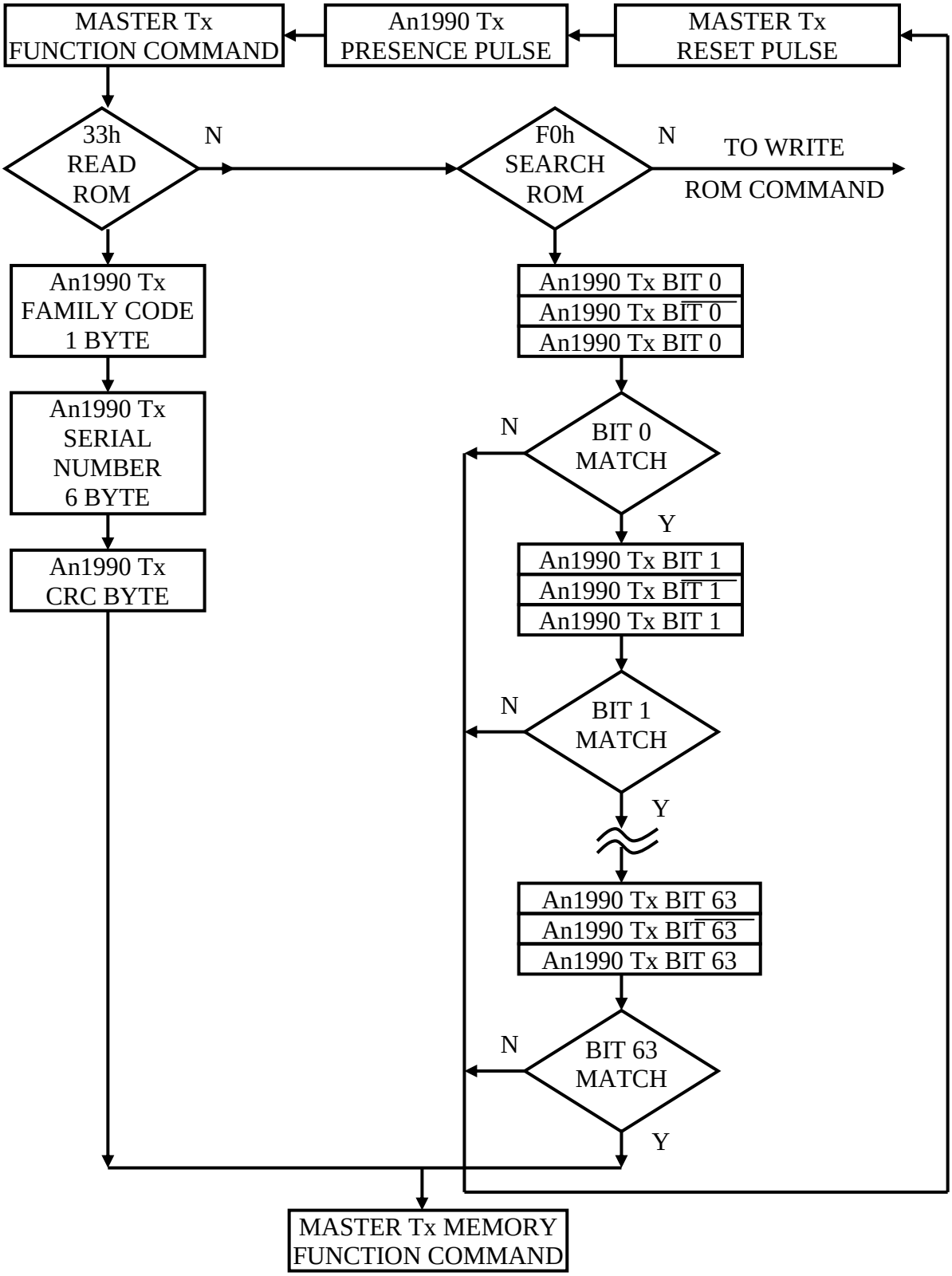
ROM FUNCTION FLOW CHART (Figure 6)



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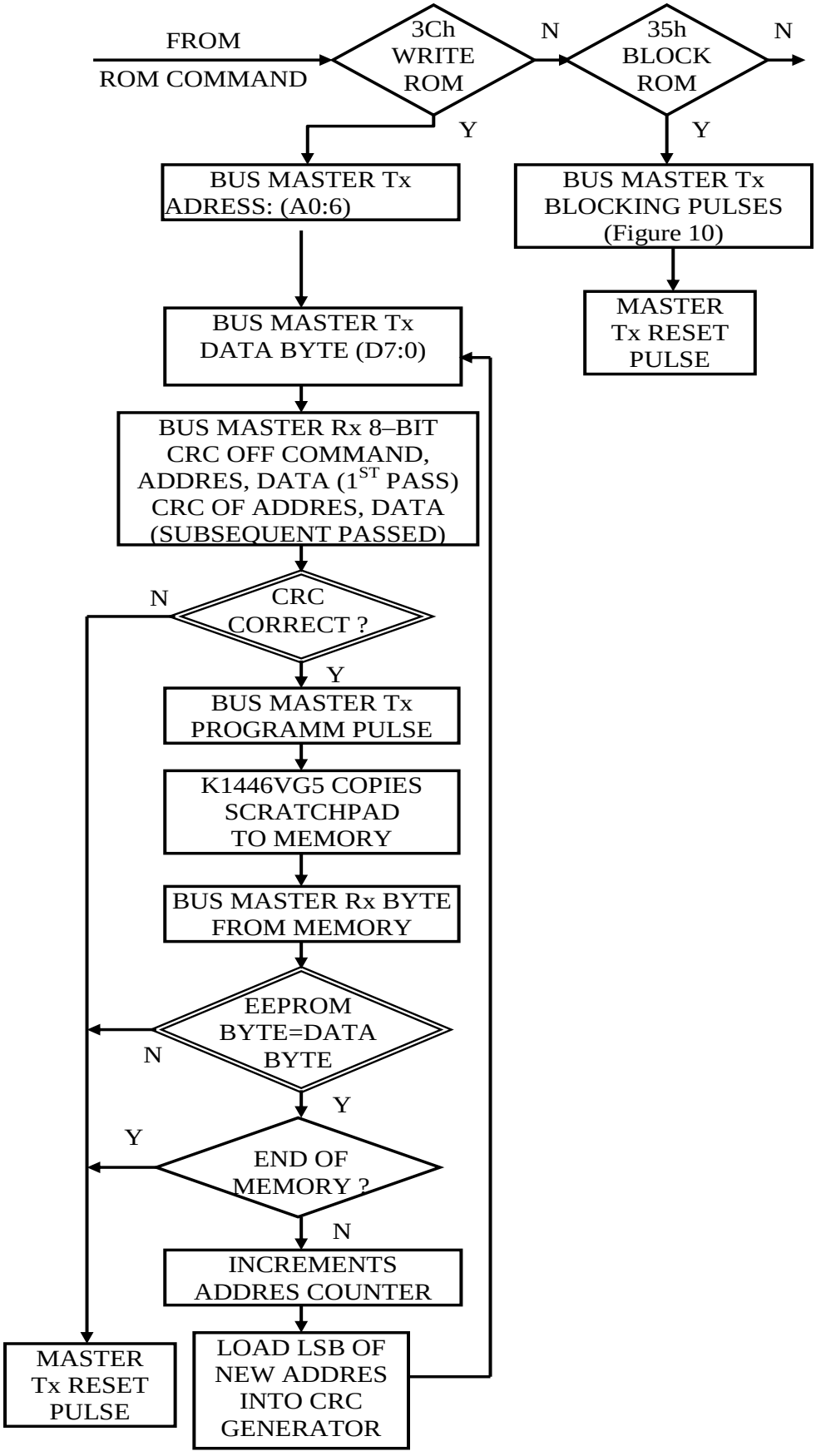
ROM FUNCTION FLOW CHART (continued Figure 6)



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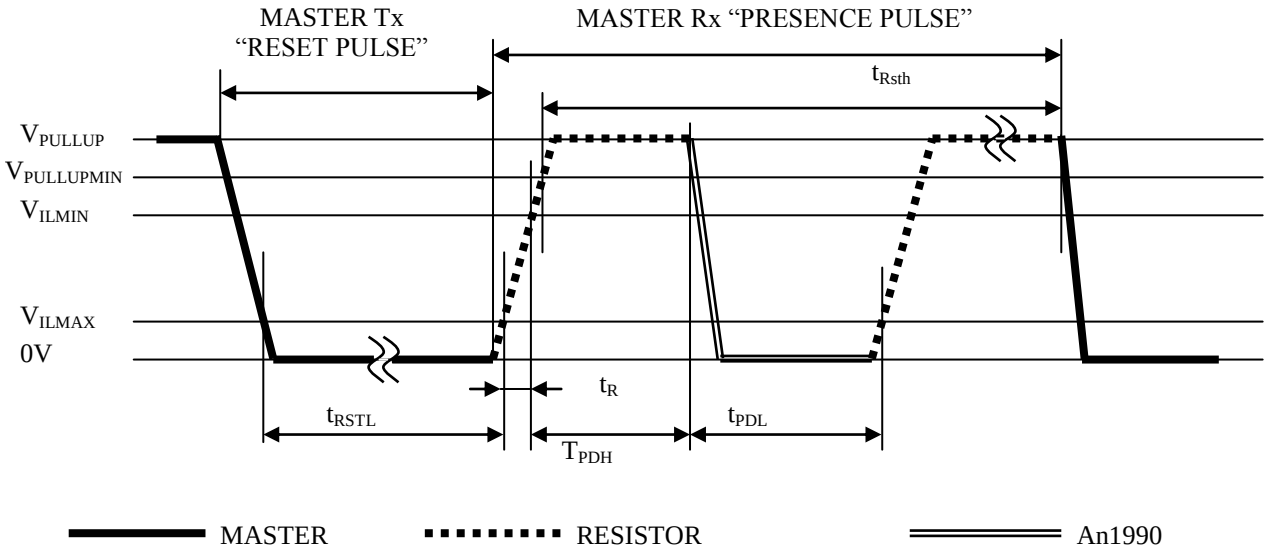
1-Wire Signaling

The AN1990 requires strict protocols to insure data integrity. The protocol consists of six types of signalling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data, Program Pulse and Blocking Pulse. All these signals except presence pulse are initiated by the bus master. The initialisation sequence required to begin any communication with the AN1990 is shown in Figure 10. A Reset Pulse followed by a Presence Pulse indicates the AN1990 is ready to accept a ROM command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pull-up resistor. After detecting the rising edge on the data pin, the AN1990 waits (t_{PDH}, 15…60 us) and then transmits the presence pulse (t_{PDL}: 60…160us).

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSE" (Figure 7)



Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 8. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the AN1990 to the master by triggering a delay circuit in the AN1990. During write time slots, the delay circuit determines when the AN1990 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the AN1990 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the device will leave the read data time slot unchanged.

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READ/WRITE TIMING DIAGRAM (Figure 8)

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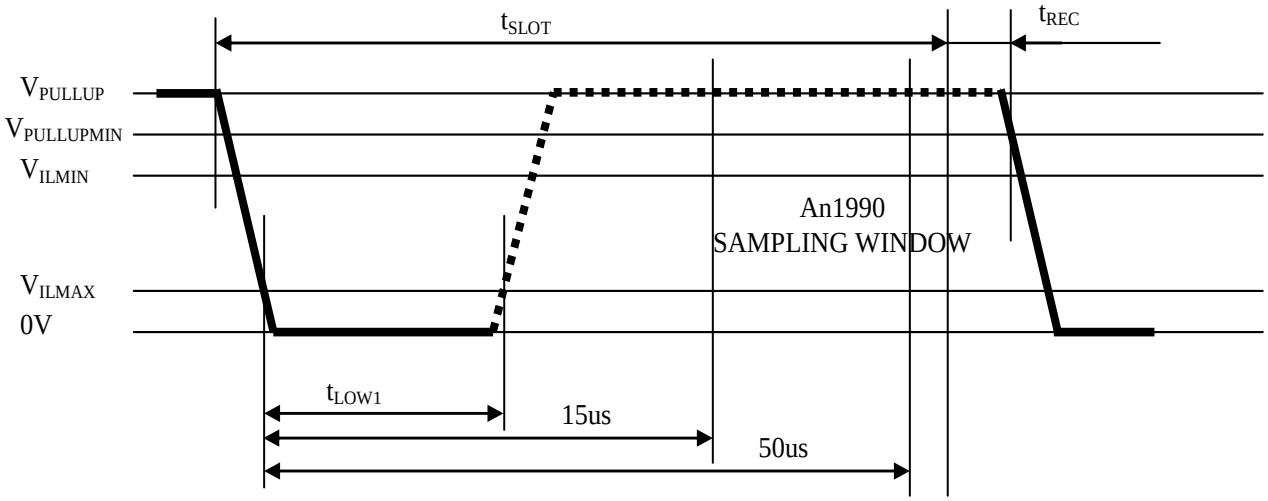
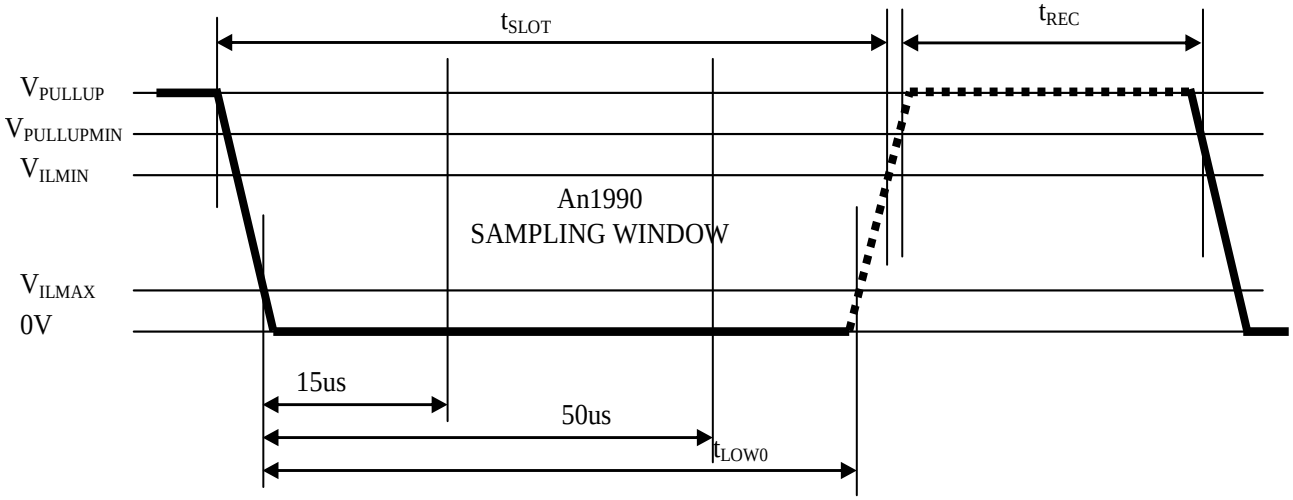
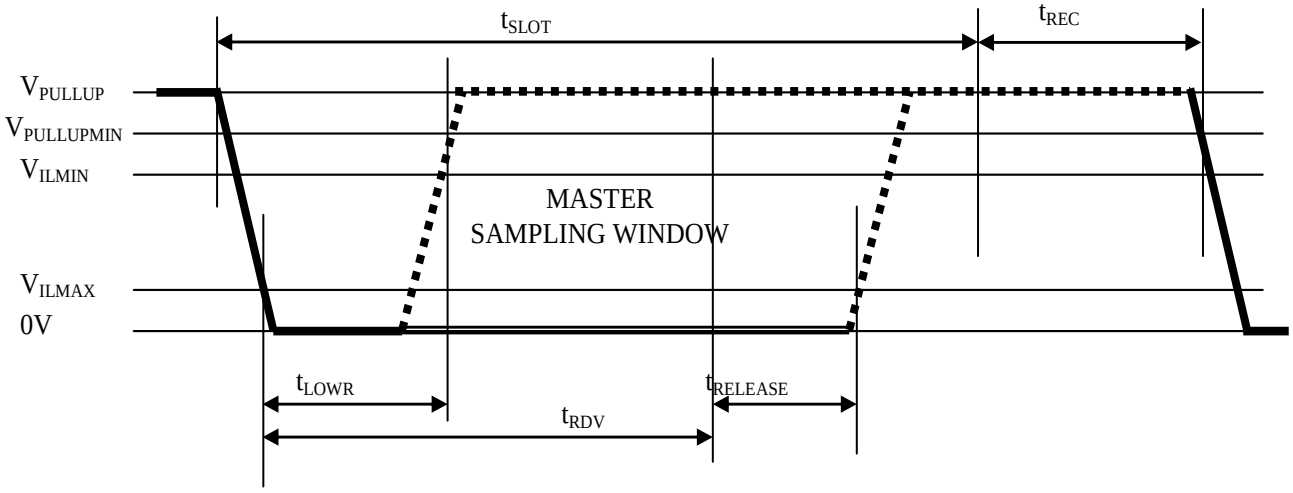
Write–one Time Slot



Write–ziro Time Slot



Read Data Time Slot



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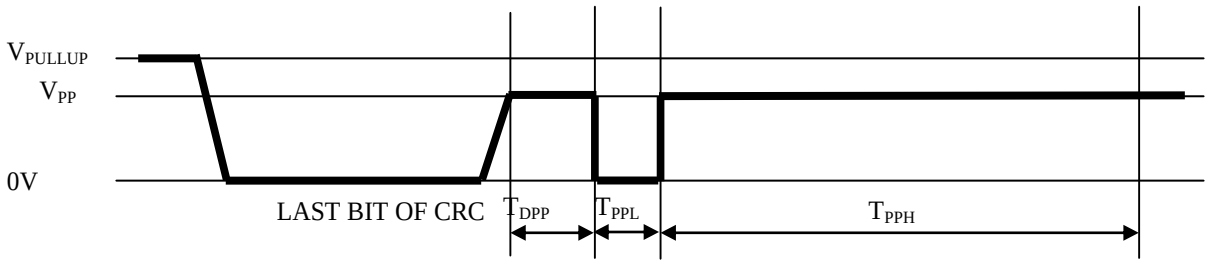
PROGRAM PULSE

To copy data from the 8-bit scratchpad to the 64-bit EEPROM Memory or Status Memory, a program pulse (Figure 9) is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct.

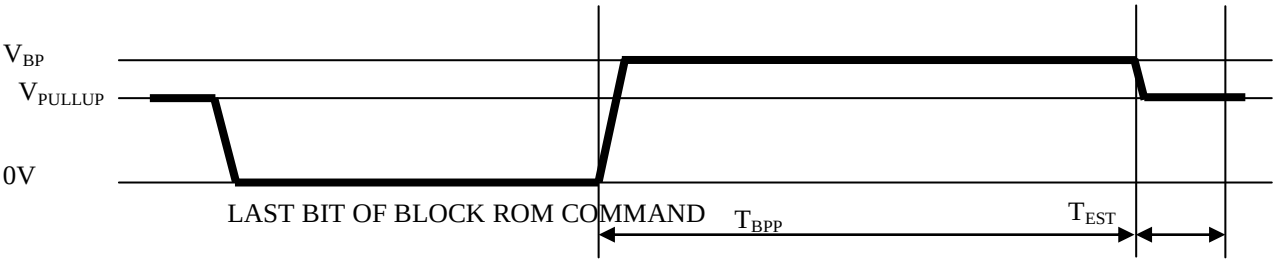
PROGRAM PULSE TIMING DIAGRAM (Figure 9)



BLOCKING PULSE

To ensure a write protection of 64-bit number Blocking pulse (Figure 10) is used. During this Blocking pulse 8V voltage is applied to the bus for 100ms.

BOLCKING PULSE TIMING DIAGRAM (Figure 10)



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ABSOLUTE MAXIMUM RATINGS*

Parameter	Value
Voltage on any Pin Relative to Ground	-0.5V to+12.0V
Operating Temperature	**-10°Cto+70°C**

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ELECTRICAL CHARACTERISTICS (VPUP =2.8V to 5.3V; -10°C to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Input Logic 1	V_{IH}	2.4		V_{CC}+0.3	V	1,4
Input Logic 0	V_{IL}	-0.3		+0.8	V	1,6
Output Logic Low @ 4mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	5.3	V	1,2
Programming Voltage	V_{PP}	4.0		4.5	V	
Data (1-Wire)	C_{IN}/OUT			800	pF	5
Burn Voltage	V_{BP}		11		V	
Current consumption			10	30	µA	

AC ELECTRICAL CHARACTERISTICS REGULAR SPEED

(VPUP =2.5V to 5.3V; -10°C to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Time Slot	**t_{SLOT}**	**50**		**120**	**us**	
Write 1 Low Time	**t_{LOW1}**	**4**		**15**	**us**	
Write 0 Low Time	**t_{LOW0}**	**40**		**120**	**us**	
Read Data Valid	t_{RDV}		15		us	
Release time	$t_{RELEASE}$	0	15	35	us	
Recovery Time	**t_{REC}**	**10**			**us**	
Reset Time High	t_{RSTH}	480			us	3
Reset Time Low	t_{RSTL}	360			us	
Presence Detect High	t_{PDH}	15		60	us	
Presence Detect Low	**t_{PDL}**	**60**		**160**	**us**	
Delay Program Pulse	t_{DPP}	600			us	
Program Pulse High	t_{PPH}	50			ms	
Program Pulse Low	t_{PPL}	5			us	
Burn Pulse High	t_{BPP}	100			ms	
Establishment Time	t_{EST}	4			us	

Notice: differences from DS1990A are marked with color.

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull-up voltage.
3. An additional reset or communication sequence cannot begin until the reset high time has expired.
4. V_{IH} is a function of the external pull-up resistor and the V_{CC} supply.
5. Capacitance on the data pin could be 800 pF when power is first applied. If a 1kOhm resistor is used to pull up the data line to V_{CC}, 5 us after power has been applied the parasite capacitance will not affect normal communications.
6. Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.

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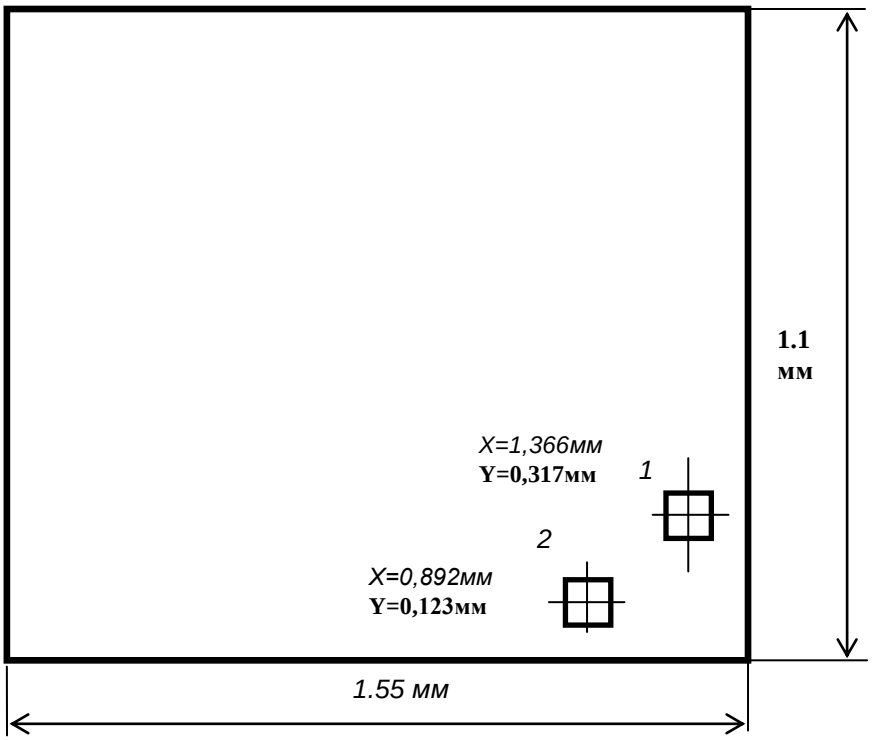
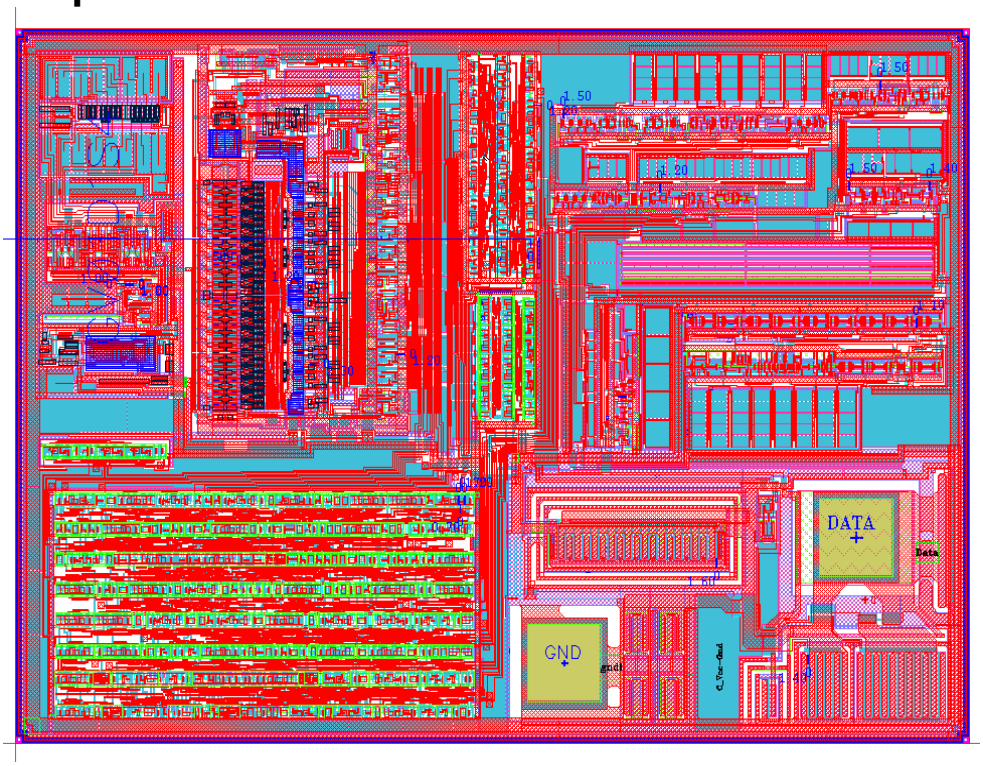
PAD DIAGRAM



Chip size 1.63 x 1.18mm with scribe line

Chip Photo



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