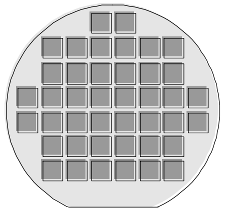

Chips or wafers

INTRODUCTION

The model An7743 are 160-output common (low) drivers of low output resistance prepared for driving the dot matrix liquid crystal panel of significantly large capacity and is to be used in combination with An7742.

The driver is featured by wide range of liquid crystal drive voltage, LCD display of high quality and chip layout ,long from side to side to minimize the LCD panel. It offers a wide range of application/

FEATURES

- The number of LCD drive outputs 160 (80x2)
- Logic system power source ....3.0 to 5.5V
- Common output on resistance……………………1K (Typ.)
- High-duty drive available 1/480
- Chip configuration long from side to side
- Unbiased display off function
- Pin select in the output shift direction available
- Adjustable offset bias of the liquid crystal according to the V_{DDH}
- Liquid Crystal drive in wide range of voltage ……….14 to 30V

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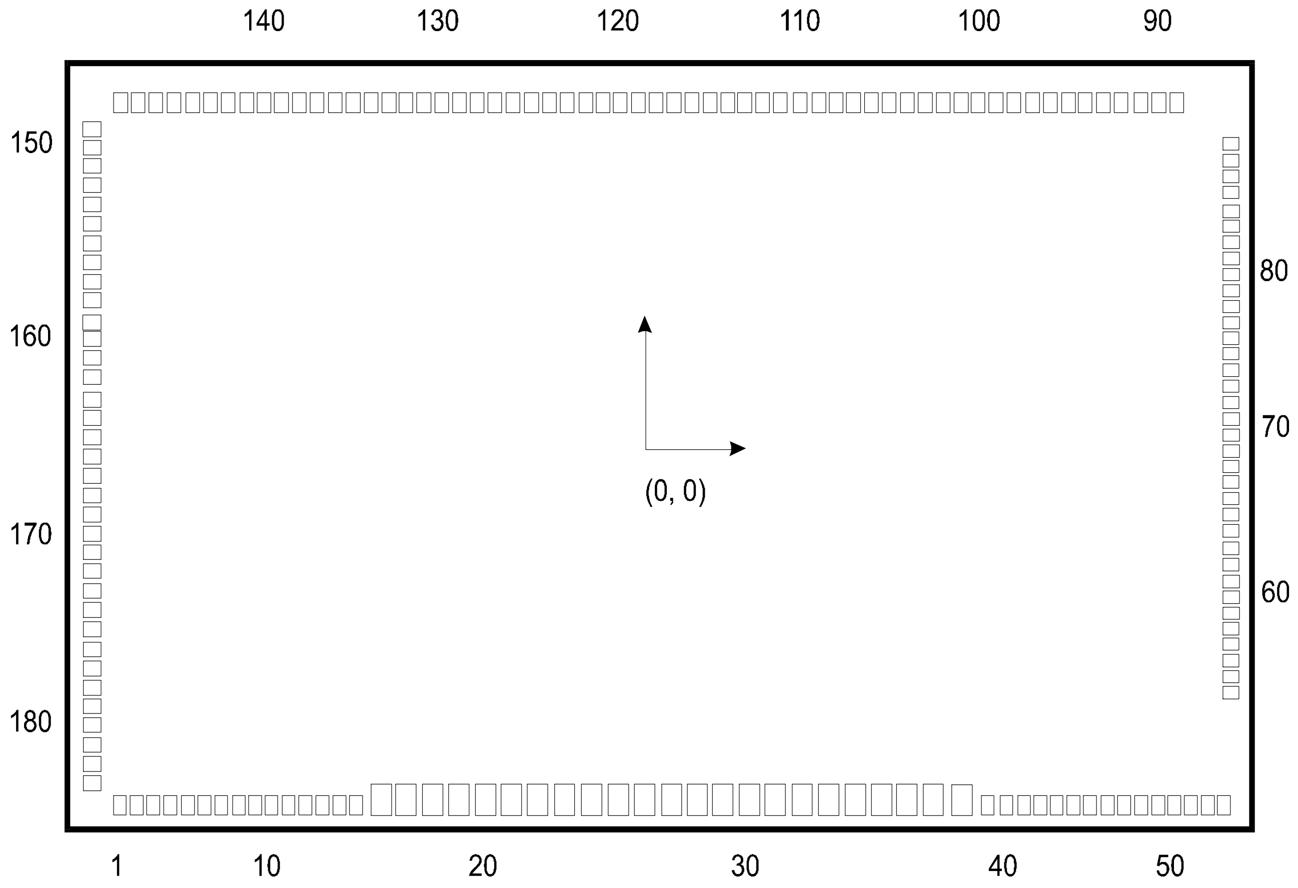
PAD DIAGRAM



Chip size: 7.30 x 4.48

Chip thickness: 470∓25µm

Pad pitch: 108 µm (Min.)

Size A: 94 x 134 ∓ 20 µm (pads 1 to 15, 39 to 183)

Size B: 115 x 148 ∓ 20 µm (pads 16 to 33 and 38)

Size C: 115 x 134 ∓ 20 µm (pads 34 to 37)

PAD LOCATION

Pad N°	Pad name	X	Y	Pad N°	Pad name	X	Y	Pad N°	Pad name	X	Y
1	O145	-3228	-2064	62	O23	3474	-975	123	O84	-487	2064
2	O146	-3120	-2064	63	O24	3474	-866	124	O85	-596	2064
3	O147	-3012	-2064	64	O25	3474	-758	125	O86	-704	2064
4	O148	-2903	-2064	65	O26	3474	-650	126	O87	-812	2064
5	O149	-2795	-2064	66	O27	3474	-542	127	O88	-921	2064
6	O150	-2687	-2064	67	O28	3474	-433	128	O89	-1029	2064
7	O151	-2578	-2064	68	O29	3474	-325	129	O90	-1137	2064
8	O152	-2470	-2064	69	O30	3474	-217	130	O91	-1245	2064
9	O153	-2362	-2064	70	O31	3474	-108	131	O92	-1354	2064
10	O154	-2253	-2064	71	O32	3474	0	132	O93	-1462	2064
11	O155	-2145	-2064	72	O33	3474	108	133	O94	-1570	2064
12	O156	-2037	-2064	73	O34	3474	217	134	O95	-1679	2064
13	O157	-1929	-2064	74	O35	3474	325	135	O96	-1787	2064
14	O158	-1820	-2064	75	O36	3474	433	136	O97	-1895	2064

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Pad N°	Pad name	X	Y	Pad N°	Pad name	X	Y	Pad N°	Pad name	X	Y
15	O159	-1712	-2064	76	O37	3474	542	137	O98	-2004	2064
16	EIO2	-1550	-2058	77	O38	3474	650	138	O99	-2112	2064
17	EIO1	-1417	-2058	78	O39	3474	758	139	O100	-2220	2064
18	GND	-1284	-2058	79	O40	3474	866	140	O101	-2328	2064
19	D0	-1151	-2058	80	O41	3474	975	141	O102	-2437	2064
20	D1	-1018	-2058	81	O42	3474	1083	142	O103	-2545	2064
21	D2	-885	-2058	82	O43	3474	1191	143	O104	-2653	2064
22	D3	-752	-2058	83	O44	3474	1300	144	O105	-2762	2064
23	NC	-619	-2058	84	O45	3474	1408	145	O106	-2870	2064
24	NC	-486	-2058	85	O46	3474	1516	146	O107	-2978	2064
25	NC	-353	-2058	86	O47	3474	1625	147	O108	-3087	2064
26	NC	-220	-2058	87	O48	3474	1733	148	O109	-3195	2064
27	SHL	-87	-2058	88	O49	3474	1841	149	O110	-3474	1841
28	XSCL	46	-2058	89	O50	3195	2064	150	O111	-3474	1733
29	TEST	179	-2058	90	O51	3087	2064	151	O112	-3474	1625
30	).T	312	-2058	91	O52	2978	2064	152	O113	-3474	1516
31	LP	445	-2058	92	O53	2870	2064	153	O114	-3474	1408
32	V_{CC}	578	-2058	93	O54	2762	2064	154	O115	-3474	1300
33	FR	711	-2058	94	O55	2653	2064	155	O116	-3474	1191
34	V5	872	-2026	95	O56	2545	2064	156	O117	-3474	1083
35	V3	1034	-2026	96	O57	2437	2064	157	O118	-3474	975
36	V2	1195	-2026	97	O58	2328	2064	158	O119	-3474	866
37	V0	1357	-2026	98	O59	2220	2064	159	O120	-3474	758
38	V_{DDH}	1550	-2058	99	O60	2112	2064	160	O121	-3474	650
39	O0	1712	-2064	100	O61	2004	2064	161	O122	-3474	542
40	O1	1820	-2064	101	O62	1895	2064	162	O123	-3474	433
41	O2	1929	-2064	102	O63	1787	2064	163	O124	-3474	325
42	O3	2037	-2064	103	O64	1679	2064	164	O125	-3474	217
43	O4	2145	-2064	104	O65	1570	2064	165	O126	-3474	108
44	O5	2253	-2064	105	O66	1462	2064	166	O127	-3474	0
45	O6	2362	-2064	106	O67	1354	2064	167	O128	-3474	-108
46	O7	2470	-2064	107	O68	1245	2064	168	O129	-3474	-217
47	O8	2578	-2064	108	O69	1137	2064	169	O130	-3474	-325
48	O9	2687	-2064	109	O70	1029	2064	170	O131	-3474	-433
49	O10	2795	-2064	110	O71	921	2064	171	O132	-3474	-541
50	O11	2903	-2064	111	O72	812	2064	172	O133	-3474	-650
51	O12	3012	-2064	112	O73	704	2064	173	O134	-3474	-758
52	O13	3120	-2064	113	O74	596	2064	174	O135	-3474	-866
53	O14	3228	-2064	114	O75	487	2064	175	O136	-3474	-975
54	O15	3474	-1841	115	O76	379	2064	176	O137	-3474	-1083
55	O16	3474	-1733	116	O77	271	2064	177	O138	-3474	-1191
56	O17	3474	-1625	117	O78	162	2064	178	O139	-3474	-1300
57	O18	3474	-1516	118	O79	54	2064	179	O140	-3474	-1408
58	O19	3474	-1408	119	O80	-54	2064	180	O141	-3474	-1516
59	O20	3474	-1300	120	O81	-162	2064	181	O142	-3474	-1625
60	O21	3474	-1191	121	O82	-271	2064	182	O143	-3474	-1733
61	O22	3474	-1083	122	O83	-379	2064	183	O144	-3474	-1841

Note : (0,0) is centre in the chip

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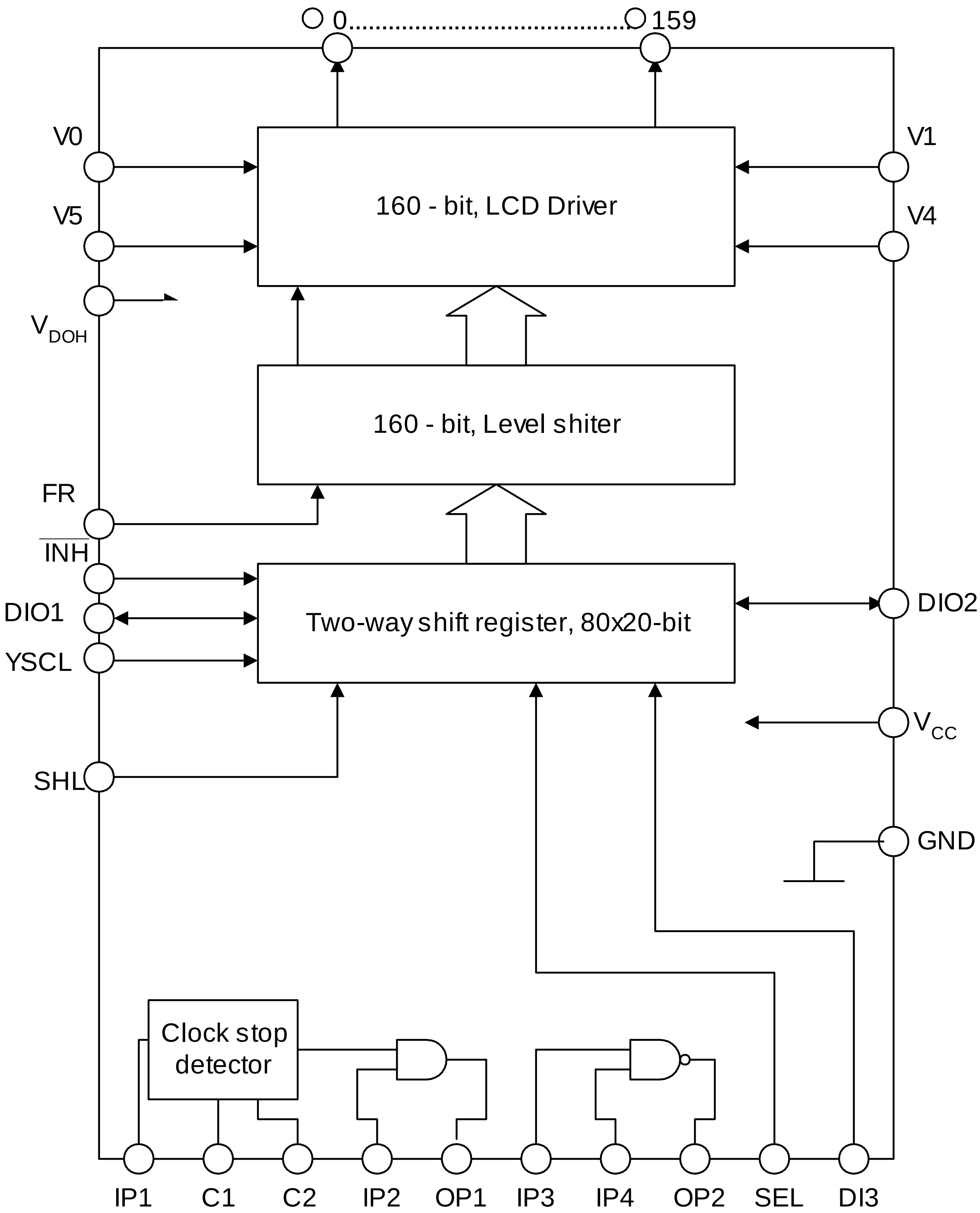
BLOCK DIAGRAM

An7743



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PIN DESCRIPTION

<table>
<tr><th>Code</th><th>I/O</th><th>Function</th><th></th></tr>
<tr><td>O 09 to 159</td><td>O</td><td>Common (low) output for liquid crystal drives. Varies at the YSCL trailing edge.</td><td>160</td></tr>
<tr><td>DIO1, DIO2</td><td>I/O</td><td>80x2-bit two-way shift register scan pulse SHL input sets the terminal to input or output. The output varies at the YSCL trailing edge. The DI3 is the input terminal of the scan pulse when 80x2 configuration is used.</td><td>3</td></tr>
<tr><td>SEL</td><td>I</td><td>Two-way shift register operation mode selection input.</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input. The scan data is shifted at the trailing edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO terminal I/O control input
<table>
<tr><td rowspan="2">SHL</td><td rowspan="2">0 Output shift direction</td><td colspan="2">DIO</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>L</td><td>0…………………………………………..159</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>159……………………………………………0</td><td>Output</td><td>Input</td></tr>
</table>
</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Input of signal to AC electrify the liquid crystal drive output</td><td>1</td></tr>
<tr><td>V_{CC}, GND</td><td>Power source</td><td>Logic power source GND V_{CC} +3V, +5V</td><td>2</td></tr>
<tr><td>V0, V1
V4, V5.
V_{DDH}</td><td>Power source</td><td>Liquid Crystal drive power source
V_{DDH}: 14V to 30V GND: 0V
$V_{DDH} \geq V0 > V1 \geq 8/9\ V_{DDH}$
$1/9V_{DDH} \geq V4 \geq V5 \geq GND$</td><td>5</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Liquid Crystal blanking control input. Low-level input sets all the common output to level.</td><td>1</td></tr>
<tr><td>IP1</td><td>I</td><td>Stop detect clock input.</td><td>1</td></tr>
<tr><td>IP2</td><td>I</td><td>Signal input to be AND-ed with the stop detect output, equipped with a pull-down resistor.</td><td>1</td></tr>
<tr><td>C1</td><td>O</td><td>1 st charge hold terminal, Capacitor extemally mounted between GND.</td><td>1</td></tr>
<tr><td>C2</td><td>O</td><td>2 nd charge hold terminal, Capacitor and resistor extemally mounted between GND.</td><td>1</td></tr>
<tr><td>OP1</td><td>O</td><td>Clock stop detect output.</td><td>1</td></tr>
<tr><td>IP4</td><td>I</td><td>NAND gate input, equipped with a pull-down resistor</td><td>1</td></tr>
<tr><td>IP4</td><td>I</td><td>NAND gate input.</td><td>1</td></tr>
<tr><td>OP2</td><td>O</td><td>NAND gate output.</td><td>1</td></tr>
</table>

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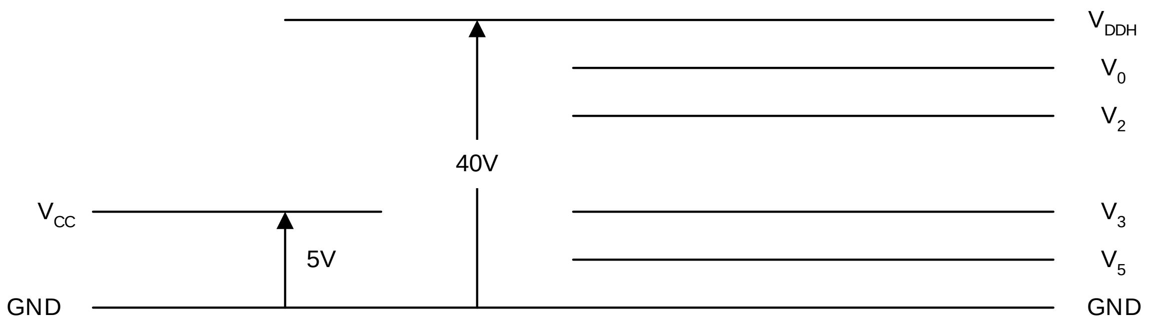
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power source voltage (1)	V_{CC}	-0.3 to +7.0	V
Power source voltage (2)	V_{DDH}	-0.3 to +45.0	V
Power source voltage (3)	V_D,V_2, V_3, V_5	GND -0.3 to V_{DDH} +0.3	V
Input voltage	V_I	GND -0.3 to V_{CC} +0.3	V
Output voltage	V_0	GND -0.3 to V_{CC} +0.3	V
EIO output current	I_{01}	20	mA
Operation temperature	Topr	-20 to +75	°C
Temperature When stored 1	Tstg1	-65 to +150	°C
Temperature When stored 2	Tstg2	-55 to +150	°C



Notes:

1. The voltage is based at GND=OV.
2. The Storage temperature 1 is specified for s single chip and the temperature 2 is for TCP mounting.
3. Voltage V0, V1 and V4 should be kept to satisfy the condition V_{DDH} V0 V1 V4 V5 GND.
4. The LSI may be eternally broken if the logic system power source floats or decreases below V_{CC}==2.9V while voltage is applied to the liquid crystal drive system power source.

Special care should be taken for the power source sequence when turning on and off the system power.

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ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics

(Unless otherwise specified, GND=V5=0V, Vcc=+5.0V ±10%, Ta=- 20 to 75°C)

Characteristic	Symbol	Condition		Pin	Min	Typ	Max	Unit
Power source voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Operation voltage recommended	V_{DDH}			V_{DDH}	14.0		30.0	V
Operation available voltage	V_{DDH}	Function		V_{DDH}	8.0			V
Power source voltage (2)	V_0	Value recommended		V_0	V_{DDH} –2.5		V_{DDH}	V
Power source voltage (3)	V_1	Value recommended		V_1	8/9V_{DDH}			V
Power source voltage (4)	V_4, V_5	Value recommended		V_4, V_5	GND		1/9V_{DDH}	V
High level input voltage	V_{IH}	V_{CC}=3.0 to 5.5V		DIO1,DIO2,DI3, IP1 to 4, SEL, FR, YSCL,SHL, INH	0.8V_{CC}			V
Low level input voltage	V_{IL}						0.2V_{CC}	V
High level input voyage	V_{OH}	V_{CC}=3.0 to 5.5V	I_{OH}=0.3mA	DIO1, DIO2, OP1, OP2	V_{CC} –0.4			V
Low level input voyage	V_{OL}		I_{OL}=0.3mA				0.4	V
Input leak current	I_{LI}	GND V_{IN} V_{CC}		DI3, SEL, FR,YSCL, SHL, INH			2.0	μA
I/O leak current	$I_{LI/O}$	GND V_{IN} V_{CC}		DIO1,DIO2	40	80	180	μA
Static current	I_{GND}	V_{DDH}=14.0 to 30.0V V_{IH}=V_{CC}, V_{IL}=GND		GND			25	μA
Output resistance	R_{SEG}	ΔV_{ON}=0.5V Condition recommended	V_{DDH}=+30.0V	O0 to O159		1.0	2.3	KΩ
			V_{DDH}=+20.0V			1.2	2.8	
Average operation current consumed (1)	I_{CC}	V_{CC}=+5.0, V_{IN}=V_{CC}, V_{IL}=GND f_{XSCL}=33.6kHz, f_{FR}=70Hz, Input data: 1/480, No load		V_{CC}		9	20	μA
		V_{CC}=+3.0V Other condition: Same as V_{CC}=5V				6	10	
Average operation current consumed (2)	I_{DDH}	V_{DDH}=V0=+30.0V, V_1=+28.0V, V_5=+0.0V, V_{CC}=+5.0V, V_4=+2.0V Other condition: Same as Icc		V_{DD}		18	40	μA
Input terminal capacity	C_I	Freq.=1MHz Ta =25°C Single chip		DI3,IP1 to 4,SEL, FR,YSCL,SHL, INH			8	pF
I/O terminal capacity	$C_{I/O}$			EIO1,EIO2			15	pF

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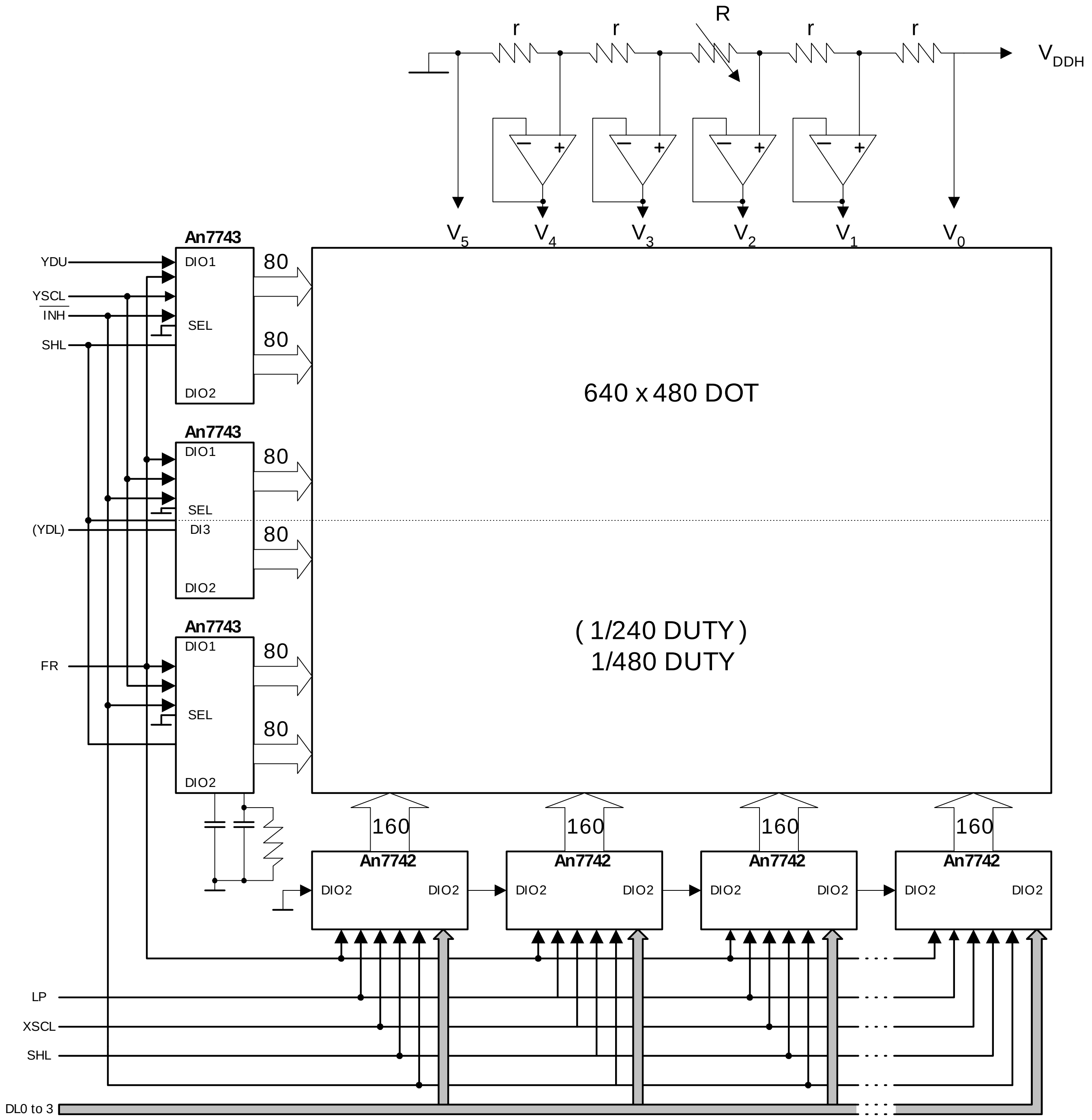
CIRCUIT DIAGRAM FOR REFERENCE

Combination of An7742 with An7743



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