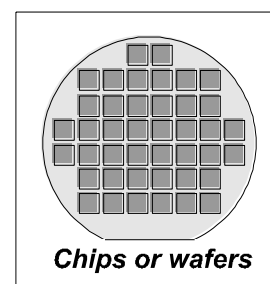




120-Channel STN LCD Driver

DESCRIPTION

An6812 is a 120-output segment/common driver IC suitable for driving small or medium scale dot matrix LCD panels. An6812 is good as a segment driver, a common driver or a common/segment driver, and it can create low power consumption, high-resolution LCD. The An6812 have eight modes can selected to set common and segment numbers by select register. The An6812 also have analog DC/DC converter used. This driver IC is very suitable for ELA, PDA or electronic dictionary.



FEATURES

Number of output channels: 120

- Maximum output voltage of driver channel: **25.0V**
- Supply voltage for the logic system: 2.4V ~ 5.0V
- Low power consumption and Low out impedance
- Low power liquid crystal display power supply circuit equipped internally Booster circuit (with Boost ratio of 2X/3X/4X/5X/6X)

Regulator circuit

Follower circuit

- Display duty selectable by internal select register

| EV3! | EV2! | EV1! | EVUZ! |
|------|------|------|-------|
| 0 | 0 | 0 | -- |
| 0 | 0 | 1 | 1/32 |
| 0 | 1 | 0 | 1/48 |
| 0 | 1 | 1 | 1/64 |
| 1 | 0 | 0 | 1/80 |
| 1 | 0 | 1 | 1/96 |
| 1 | 1 | 0 | 1/112 |
| 1 | 1 | 1 | 1/120 |

- Package
 - 160-pin QFP
 - 154-pin COB

In the Segment mode

- Maximum shift clock frequency
 - 20MHz @ 5.0V
 - 16MHz @ 3.0V ~ 5.0V
 - 12MHz @ 2.4V ~ 5.0V
- Data input interface (pin option)
 - 4-bit parallel mode
 - 1-bit serial mode
- Automatic transfer function
- Data latch circuit are reset when DISPOFF active

In the Common mode

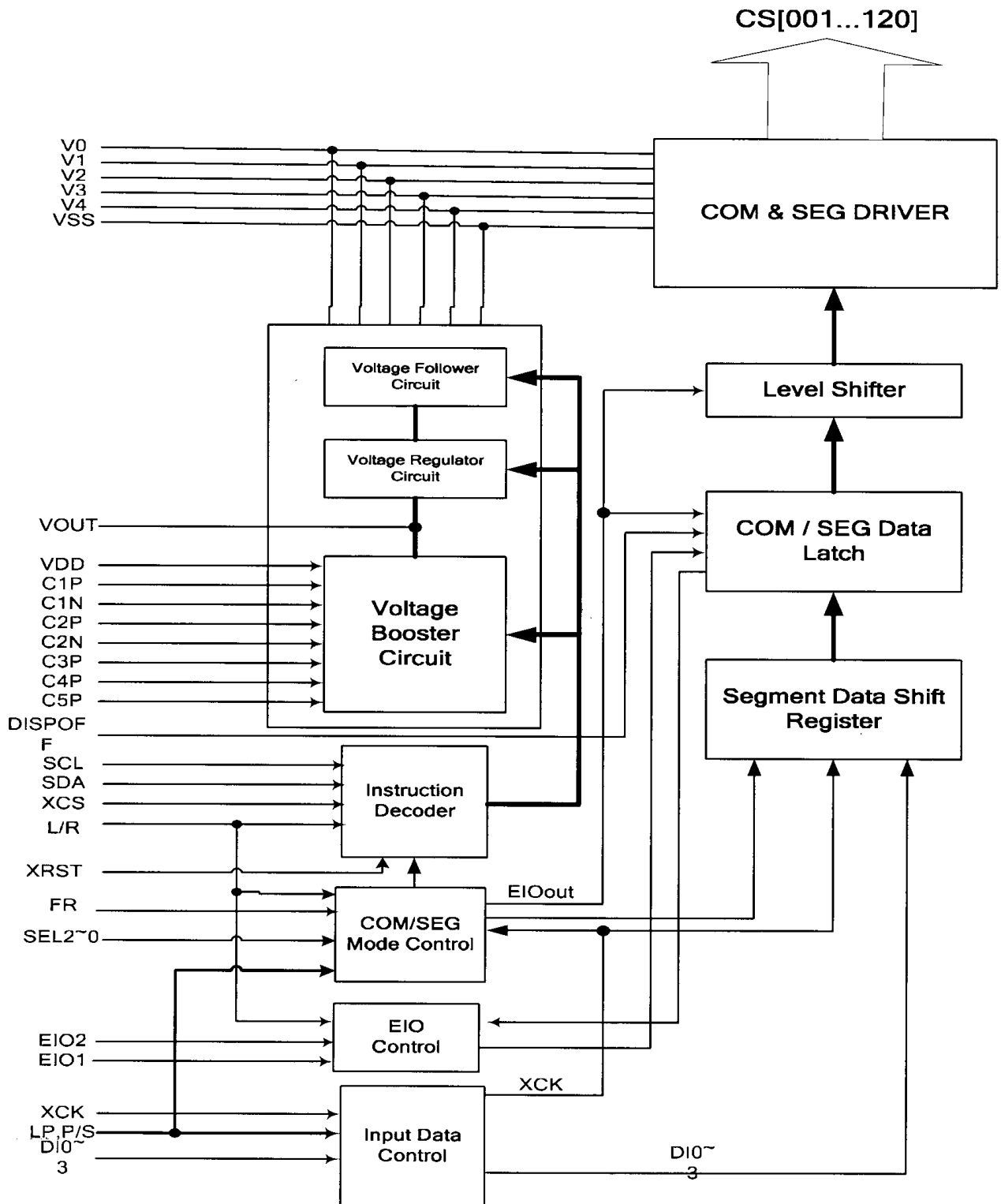
- Maximum shift clock frequency
 - 4MHz
- Built-in N-bit shift register
- Shift register circuit are reset when DISPOFF active

**PAD DESCRIPTION**

| Symbol | Type | Description | No of Num | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|------|--|-----------|--------------|-----|------|------|---|---|---|----|--------------|---|---|---|------|------------|---|---|---|------|------------|---|---|---|------|------------|---|---|---|------|------------|---|---|---|------|-------------|---|---|---|-------|-------------|---|---|---|-------|-------------|---|
| VDD | P | Positive power supply for logic system (2.4V ~ 5.0V) | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | P | Ground (0V) | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V0,V1,V2,V3,V4 | P | Power supply for LCD driver (V0 .V1 .V2 .V3 .V4) | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DI0 ~ DI3 | I | Display data input | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| EIO1, EIO2 | I/O | Input/output for chip selection at segment mode and FLM input/output function at com/seg mix mode or common mode 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| XCK | I | Serial clock input for taking display data at segment mode | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| FR | I | Polarity signal input for LCD driving waveform | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LP | I | Latch pulse input for display data at segment mode and/or shift pulse input at common mode. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L/R | I | Select the shift register direction. When set to low (GND), the data is shifted from CS001 to CS120. When set to high (VDD), the data is shifted from CS120 to CS001 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DISPOFF | I | Control input pin to fix the driver output(SC001~SC120) to GND level. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C1P | O | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C1N | O | DC/DC voltage converter charge-pump pulse output. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C2P | O | DC/DC voltage converter. Connect a capacitor between this terminal and the C2N terminal. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C2N | O | DC/DC voltage converter charge-pump pulse output. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C3P | O | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C4P | O | DC/DC voltage converter. Connect a capacitor between this terminal and the C2N terminal. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C5P | O | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VOUT | O | DC/DC voltage converter. Connect a filter capacitor between this terminal and GND. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TEST1, TEST2 | I | Test pins (for test mode only). | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CS001~CS120 | O | LCD driving output. | 120 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SCL | I | Serial clock line (CPU interface). | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SDA | I | Serial data line (CPU interface). | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| XCS | I | Chip Select Input, active low (CPU interface). | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| XRST | I | Chip Reset Input, active low. | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DU2~DU0 | I | <p>These pins are for DUTY selection.</p> <table border="1"> <thead> <tr> <th>DU2</th> <th>DU1</th> <th>DU0</th> <th>DUTY</th> <th>BIAS</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>--</td> <td>Segment Mode</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1/32</td> <td>1/6 or 1/5</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1/48</td> <td>1/7 or 1/5</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1/64</td> <td>1/9 or 1/7</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1/80</td> <td>1/9 or 1/7</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1/96</td> <td>1/10 or 1/8</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1/112</td> <td>1/11 or 1/9</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1/120</td> <td>1/11 or 1/9</td> </tr> </tbody> </table> | DU2 | DU1 | DU0 | DUTY | BIAS | 0 | 0 | 0 | -- | Segment Mode | 0 | 0 | 1 | 1/32 | 1/6 or 1/5 | 0 | 1 | 0 | 1/48 | 1/7 or 1/5 | 0 | 1 | 1 | 1/64 | 1/9 or 1/7 | 1 | 0 | 0 | 1/80 | 1/9 or 1/7 | 1 | 0 | 1 | 1/96 | 1/10 or 1/8 | 1 | 1 | 0 | 1/112 | 1/11 or 1/9 | 1 | 1 | 1 | 1/120 | 1/11 or 1/9 | 3 |
| DU2 | DU1 | DU0 | DUTY | BIAS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | -- | Segment Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1/32 | 1/6 or 1/5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1/48 | 1/7 or 1/5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1/64 | 1/9 or 1/7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1/80 | 1/9 or 1/7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1/96 | 1/10 or 1/8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1/112 | 1/11 or 1/9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1/120 | 1/11 or 1/9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

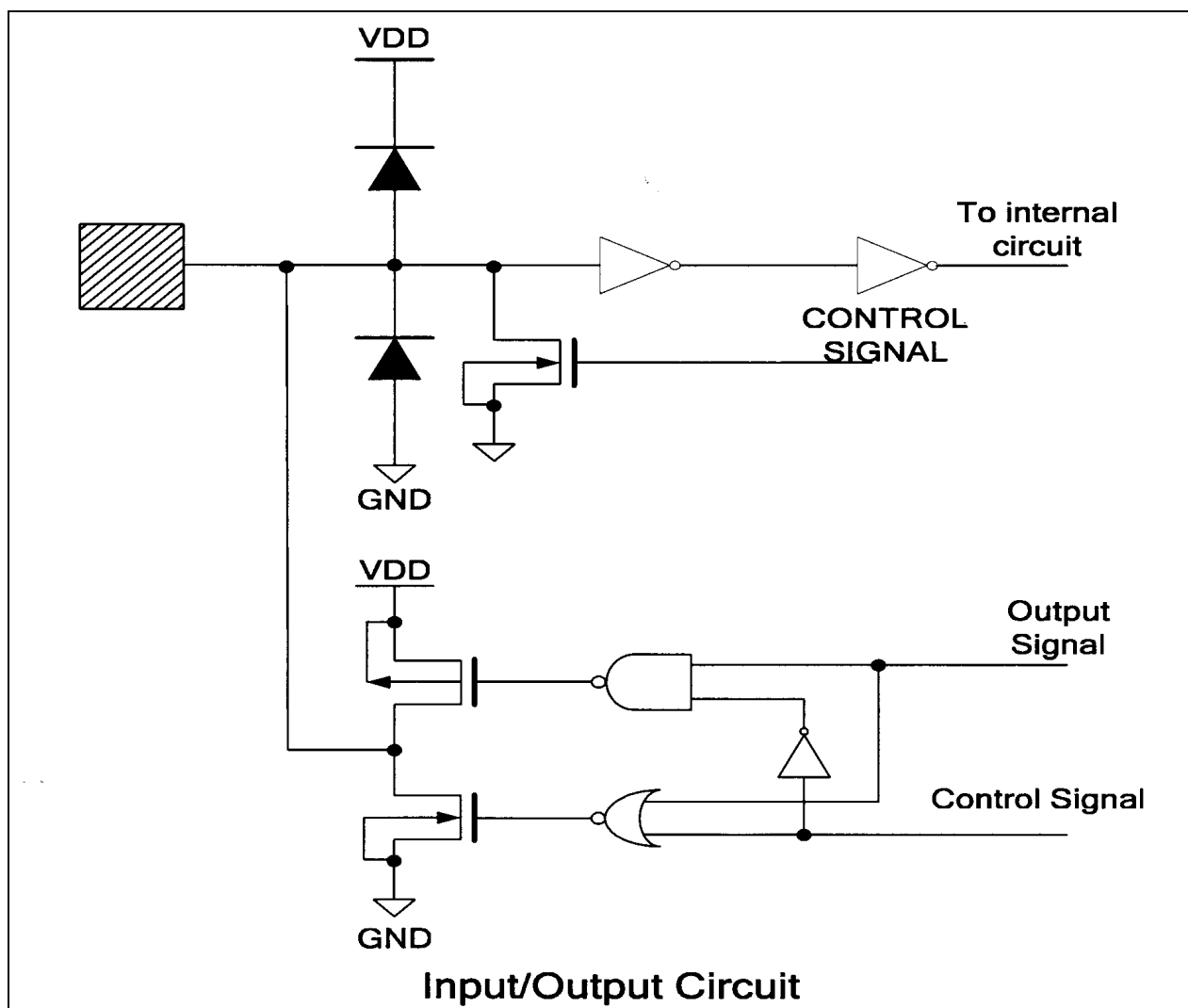
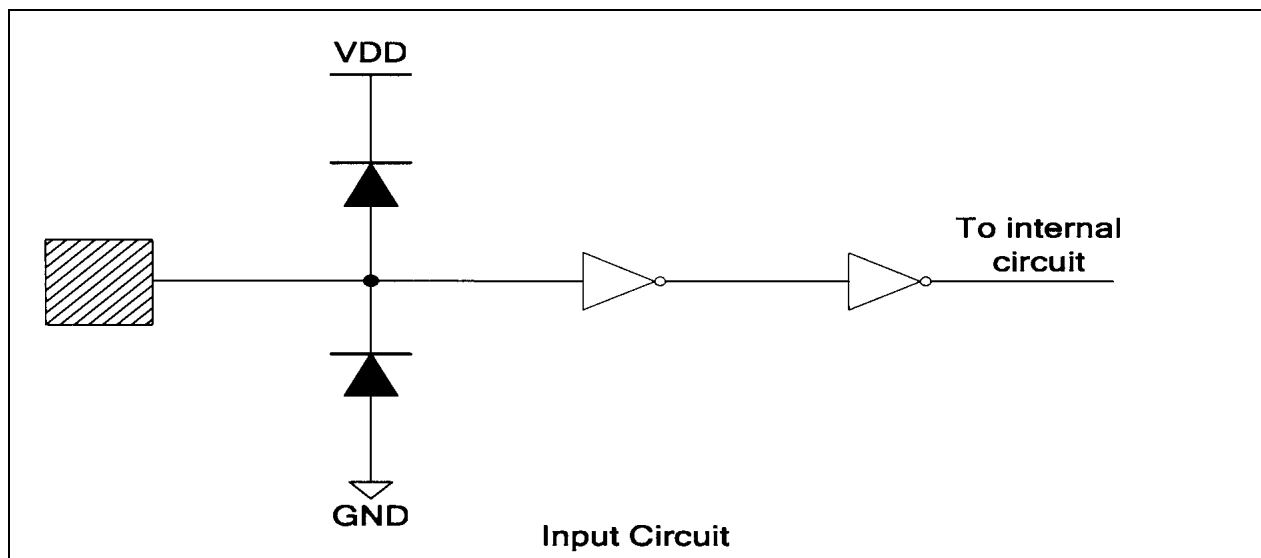


BLOCK DIAGRAM





INPUT / OUTPUT CIRCUIT





Functional Description

In the Common mode

| Symbol | Function |
|--------------------|---|
| VDD | Power supply pin for logic system, connect to 2.4V ~ 5.0V |
| GND | Ground pin, connect to 0V |
| V0,V1,V2, V3,V4 | Power supply pins for STN LCD driver, the supplied voltage is determined by the specification of LCD panel. Usually, the voltage is changed via the resistive voltage divider or changing impedance of operational amplifier. Voltage levels are determined based on GND and must maintain the relative magnitudes shown below. $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq GND$. When the voltage regulator turns ON, the internal power supply circuits produce the V0 voltage. When the followers turns ON, the internal power supply circuits produce the V1 to V4 voltages. The voltage settings are selected by instruction or keep default state if MCU interface is not used. |
| DI0~3 | Not used. (Connect DI3-DI0 to GND or VDD.) |
| XCK | Not used. XCK will be pulled low in COMMON mode, connect to GND if possible. |
| XRST | System Reset Pin. Pull high if no use. Active low level XRST pulse should has timing min value 200us, max value 0.5s. |
| LP | Shift clock pulse input pin for bi-directional shift register. Data is shifted at the falling edge of the clock pulse. |
| L/R | Input pin for selecting the shift direction of bi-directional shift register <ul style="list-style-type: none"> L/R=0 (GND), Data are shifted from CS120 to CS001. L/R=1 (VDD), Data are shifted from CS001 to CS120. |
| DISPOFF | Control input pin for Un-Select LCD output level. <ul style="list-style-type: none"> While setting this pin to 'L' (GND), all common and segment drivers are setted to GND. The LCD driver performs as 'off' state. While setting this pin to 'H' (VDD), the common and segment drivers behave their normal display state. When set to "L", the contents of the shift register are reset to not reading data. When the DISPOFF function is canceled, the driver outputs non-select level (V1 or V4), and the shift data is read at the next falling edge of the LP. |
| FR | Polarity input signal for LCD waveform. LCD output drivers change their polarity with FR signal. The FR signal is toggle by one frame. |
| EIO1, EIO2 | Input/output pins for chip selection <ul style="list-style-type: none"> While L/R is set to 'L' (GND), EIO1 is set as output (EO) and EIO2 is set as input (EI). EIO2 input can be connected to FLM signal of controller or EIO1 output of previos common driver IC. EIO1 output can be connected to EIO2 input of next driver IC or left open. While L/R is set to 'H' (VDD), EIO2 is set as output (EO) and EIO1 is set as input (EI). EIO1 input can be connected to FLM signal of controller or EIO2 output of previos common driver IC. EIO2 output can be connected to EIO1 input of next driver IC or left open. |
| CS001 ~ CS120 | LCD COMMON output pins at this mode. One voltage level among V0, V1, V4 and GND is selected and output and make the COMMON waveform. Their timing is based on LP and FR. |
| C1P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |
| C1N | DC/DC voltage converter charge-pump pulse output. |
| C2P | DC/DC voltage converter. Connect a capacitor between this terminal and the C2N terminal. |
| C2N | DC/DC voltage converter charge-pump pulse output. |
| C3P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |
| C4P | DC/DC voltage converter. Connect a capacitor between this terminal and the C2N terminal. |
| C5P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |
| VOUT | DC/DC voltage converter. Connect a filter capacitor between this terminal and GND. |
| SCL | The serial interface clock input. |
| SDA | The serial interface data. |
| XCS | Chip Select of LCD Driver serial interface, low active. |
| DU2 ~ 0 | DU2~0 are set to '111' (all VDD) for this mode. |

**In the Segment mode**

| Symbol | Function |
|--------------------|---|
| VDD | Power supply pin for logic system, connect to 2.4V ~ 5.0V |
| GND | Ground pin, connect to 0V |
| V0,V1,V2, V3,V4 | Power supply pins for STN LCD driver, the supplied voltage is determined by the specification of LCD panel. Usually, the voltage is changed via the resistive voltage divider or changing impedance of operational amplifier. Voltage levels are determined based on GND and must maintain the relative magnitudes shown below. $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq GND$ When the voltage regulator turns ON, the internal power supply circuits produce the V0 voltage. When the followers turns ON, the internal power supply circuits produce the V1 to V4 voltages. The voltage settings are selected by instruction or keep default state if MCU interface is not used. |
| DI0~3 | Input pins for display data. In 4-bit parallel mode (P/S='1'), data is received via DI[0..3]. In 1-bit serial mode (P/S='0'), data is received via only DI0. The other pins DI[1..3] should be connected to GND or VDD |
| XCK | Clock input for taking display data at segment mode. Data is read at the falling edge of this signal. |
| XRST | System Reset Pin. Pull high if no use. Active low level XRST pulse should has timing min value 200us, max value 0.5s. |
| LP | Latch pulse input pin for display data. Data is latched to the driver stage at the falling edge of the clock pulse. |
| L/R | Input pin for selecting the reading direction of display data. When set to 0 (GND), the data are read from CS120 to CS001. When set to 1 (VDD), the data are read from CS001 to CS120. |
| DISPOFF | Control input pin for Un-Select LCD output level. <ul style="list-style-type: none"> While setting this pin to 'L' (GND), all common and segment drivers are setted to GND. The LCD driver performs as 'off' state. While setting this pin to 'H' (VDD), the common and segment drivers behave their normal display state. While DISPOFF goes 'H' from 'L', the segment drivers don't output normal voltage levels immediately. At falling edge of next LP, the segment drivers output their normal voltage levels (V2 or V3) corresponding to latched data. |
| FR | Polarity input signal for LCD drivers waveform. LCD output drivers change their polarity with FR signal. The FR signal is toggle by one frame. |
| P/S | Segment data interface mode selection pin <ul style="list-style-type: none"> Input high (VDD) for 4-bit parallel input mode. D0~D3 are used together. Input low (GND) for 1-bit serial input mode. D0 used only, D1~D3 should connect to GND or VDD. |
| EIO1, EIO2 | Input / output pins for chip enable of automatic transfer function. While L/R is set to 'L' (GND), EIO1 is set as output (EO) and EIO2 is set as input (EI). While L/R is set to 'H' (VDD), EIO1 is set as input (EI) and EIO2 is set as output (EO). These two pins are used while only cascading two or more LCD segment drivers. While EI is set to 'L', the corresponding chip is selected and gates the display data. After receiving 120 bits data, this chip is non-selected and discards following data. The next chip then is selected by a low pulse on its EI. The selected chip will latch the incoming data and non-selected chips discard the data. Please note, the first chip's EI has to be connected to GND and other EIs are connected to their previous chips' Eos. |
| CS001 ~ CS120 | LCD segment output pins. One voltage level among V0, V2, V3 and GND is selected and output corresponding to the bit of latched data. |
| C1P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |
| C1N | DC/DC voltage converter charge-pump pulse output. |
| C2P | DC/DC voltage converter. Connect a capacitor between this terminal and the C2N terminal. |
| C2N | DC/DC voltage converter charge-pump pulse output. |
| C3P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |



| | |
|---------|--|
| C4P | DC/DC voltage converter. Connect a capacitor between this terminal and the C2N terminal. |
| C5P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |
| VOUT | DC/DC voltage converter. Connect a filter capacitor between this terminal and GND. |
| SCL | The serial interface clock input. |
| SDA | The serial interface data. |
| XCS | Chip Select of LCD Driver serial interface, low active. |
| DU2 ~ 0 | DU 2~0 are set to '000' (GND) for this mode. |

In the Common/Segment mix mode

| Symbol | Function |
|--------------------|---|
| VDD | Power supply pin for logic system, connect to 2.4V ~ 5.0V |
| GND | Ground pin, connect to 0V |
| V0, V1, V2, V3, V4 | Power supply pins for STN LCD driver, the supplied voltage is determined by the specification of LCD panel. Usually, the voltage is changed via the resistive voltage divider or changing impedance of operational amplifier. Voltage levels are determined based on GND and must maintain the relative magnitudes shown below. $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq GND$ When the voltage regulator turns ON, the internal power supply circuits produce the V0 voltage. When the followers turn ON, the internal power supply circuits produce the V1 to V4 voltages. The voltage settings are selected by instruction or keep default state if MCU interface is not used. |
| DI0 ~ 3 | Input pins for display data <ul style="list-style-type: none"> .In 4-bit parallel mode (P/S='1'), data is received via DI[0..3]. .In 1-bit serial mode (P/S='0'), data is received via only DI0. The other pins DI[1..3] should be connected to GND. |
| XCK | Clock input for taking display data <ul style="list-style-type: none"> Display data are read at the falling edge of clock pulse. |
| LP1 | Latch pulse input pin for display data <ul style="list-style-type: none"> Data are latched at the falling edge of the clock pulse. Shift clock pulse input pin for bi-directional shift register Data are shifted at the falling edge of the clock pulse. |
| DISPOFF | Control input pin for Un-Select LCD output level. <ul style="list-style-type: none"> While setting this pin to 'L' (GND), all common and segment drivers are set to GND. The LCD driver performs as 'off' state. While setting this pin to 'H' (VDD), the common and segment drivers behave their normal display state. While DISPOFF goes 'H' from 'L', the segment drivers don't output normal voltage levels immediately. At falling edge of next LP, the segment drivers output their normal voltage levels (V2 or V3) corresponding to latched data. |
| FR | Polarity input signal for LCD waveform. LCD output drivers change their polarity with FR signal. The FR signal is toggle by one frame. |
| P/S | Segment data interface mode selection pin <ul style="list-style-type: none"> Input high (VDD) for 4-bit parallel input mode. D0~D3 are used together. Input low (GND) for 1-bit serial input mode. D0 used only, D1~D3 should connect to GND or VDD. |
| EIO1, EIO2 | Input / output pins for chip selection <ul style="list-style-type: none"> While L/R is set to 'L' (GND), EIO1 is set as output (EO) and EIO2 is set as input (EI). EIO1: Segment chip enable output, as default segment is enabled internally and be non-selected after 8, 24, 40, 56, 72 or 88 bits of data have been read. Depend on select mode. EIO2: Common shift data input, no shift data output While L/R is set to 'H' (VDD), EIO1 is set as input (EI) and EIO2 is set as output (EO). EIO1: Common shift data input, no shift data output EIO2: Segment chip enable output, as default segment is enabled internally and be non-selected after 8, 24, 40, 56, 72, or 88 bits of data have been read. Depend on select mode. During output, set to "H" while LP. XCK is "H" and after 120 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". |
| CS001 ~ | LCD segment output pins |



| | |
|-------|--|
| CS120 | <ul style="list-style-type: none"> One voltage level among V0, V1, V2, V3 V4, and GND is selected and output corresponding to the bit of latched data and duty mode selected (DU2-0). |
| C1P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |
| C1N | DC/DC voltage converter charge-pump pulse output. |
| C2P | DC/DC voltage converter. Connect a capacitor between this terminal and the C2N terminal. |
| C2N | DC/DC voltage converter charge-pump pulse output. |
| C3P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |
| C4P | DC/DC voltage converter. Connect a capacitor between this terminal and the C2N terminal. |
| C5P | DC/DC voltage converter. Connect a capacitor between this terminal and the C1N terminal. |
| VOUT | DC/DC voltage converter. Connect a filter capacitor between this terminal and GND. |
| XCS | Chip Select of LCD Driver serial interface, low active.. When the command mode is not used then must fixed to VDD. |
| SCL | The serial clock interface input. |
| SDA | The serial interface data. |

Functional Operation

• In the Common Mode

| DISPOFF | FR | Latched data (bit) | Output Voltage Level |
|---------|----|--------------------|----------------------|
| H | L | L | V4 |
| H | L | H | V0 |
| H | H | L | V1 |
| H | H | H | GND |
| L | X | X | GND |

• In the Segment Mode

| DISPOFF | FR | Latched data (bit) | Output Voltage Level |
|---------|----|--------------------|----------------------|
| H | L | L | V3 |
| H | L | H | GND |
| H | H | L | V2 |
| H | H | H | V0 |
| L | X | X | GND |

Where 'L' = GND, 'H' = VDD, 'X' = Don't care. (Should be connect VDD or GND, don't floating it.)



Relationship between Display data and Data Input Pins (DI[0..3])

- IN THE SEGMENT MODE

4-bit Parallel Mode

| L/R | EIO1 | EIO2 | Data input | Clock count | | | | | | |
|-----|--------|--------|------------|-----------------------|-----------------------|-----------------------|-----|------------------------|------------------------|------------------------|
| | | | | 1 st clock | 2 nd clock | 3 rd clock | ... | 28 th clock | 29 th clock | 30 th clock |
| L | Output | Input | DI0 | CS117 | CS113 | CS109 | ... | CS009 | CS005 | CS001 |
| | | | DI1 | CS118 | CS114 | CS110 | ... | CS010 | CS006 | CS002 |
| | | | DI2 | CS119 | CS115 | CS111 | ... | CS011 | CS007 | CS003 |
| | | | DI3 | CS120 | CS116 | CS112 | ... | CS012 | CS008 | CS004 |
| H | Input | Output | DI0 | CS004 | CS008 | CS012 | ... | CS112 | CS116 | CS120 |
| | | | DI1 | CS003 | CS007 | CS011 | ... | CS111 | CS115 | CS119 |
| | | | DI2 | CS002 | CS006 | CS010 | ... | CS110 | CS114 | CS118 |
| | | | DI3 | CS001 | CS005 | CS009 | ... | CS109 | CS113 | CS117 |

1-bit Serial Mode

| L/R | EIO1 | EIO2 | Data input | Clock count | | | | | | |
|-----|--------|--------|------------|-----------------------|-----------------------|-----------------------|-----|-------------------------|-------------------------|-------------------------|
| | | | | 1 st clock | 2 nd clock | 3 rd clock | ... | 118 th clock | 119 th clock | 120 th clock |
| L | Output | Input | DI0 | CS120 | CS119 | CS118 | ... | CS003 | CS002 | CS001 |
| | | | DI1 | X | X | X | X | X | X | X |
| | | | DI2 | X | X | X | X | X | X | X |
| | | | DI3 | X | X | X | X | X | X | X |
| H | Input | Output | DI0 | CS001 | CS002 | CS003 | ... | CS118 | CS119 | CS120 |
| | | | DI1 | X | X | X | X | X | X | X |
| | | | DI2 | X | X | X | X | X | X | X |
| | | | DI3 | X | X | X | X | X | X | X |

In the Common Mode

| L/R | DATA TRANSFER DIRECTION | EIO1 | EIO2 |
|-----|-------------------------|--------|--------|
| L | CS120 → CS001 | Output | Input |
| H | CS001 → CS120 | Input | Output |

Where 'L' = GND, 'H' = VDD, 'X' = Don't care. (Should be connect VDD or GND, don't floating it.)



MIX MODE (Segment/Common mode)

IF (DU2,DU1,DU0)=(0,0,1) → Select the mode is 32 COMMON / 88 SEGMENT

• **SEGMENT SIDE OF MIX MODE**

4-bit Parallel Mode

| L/R | EIO1 | EIO2 | Data input | Clock count | | | | | | |
|-----|----------------|----------------|------------|-----------------------|-----------------------|-----------------------|-----|------------------------|------------------------|------------------------|
| | | | | 1 st clock | 2 nd clock | 3 rd clock | ... | 20 th clock | 21 th clock | 32 th clock |
| L | SEG_END Output | COM_FLM Input | DI0 | CS085 | CS081 | CS077 | ... | CS009 | CS005 | CS001 |
| | | | DI1 | CS086 | CS082 | CS078 | ... | CS010 | CS006 | CS002 |
| | | | DI2 | CS087 | CS083 | CS079 | ... | CS011 | CS007 | CS003 |
| | | | DI3 | CS088 | CS084 | CS080 | ... | CS012 | CS008 | CS004 |
| H | COM_FLM Input | SEG_END Output | DI0 | CS036 | CS040 | CS044 | ... | CS112 | CS116 | CS120 |
| | | | DI1 | CS035 | CS039 | CS043 | ... | CS111 | CS115 | CS119 |
| | | | DI2 | CS034 | CS038 | CS042 | ... | CS110 | CS114 | CS118 |
| | | | DI3 | CS033 | CS037 | CS041 | ... | CS109 | CS113 | CS117 |

1-bit Serial Mode

| L/R | EIO1 | EIO2 | Data input | Clock count | | | | | | |
|-----|----------------|----------------|------------|-----------------------|-----------------------|-----------------------|-----|------------------------|------------------------|------------------------|
| | | | | 1 st clock | 2 nd clock | 3 rd clock | ... | 62 th clock | 63 th clock | 64 th clock |
| L | SEG_END Output | COM_FLM Input | DI0 | CS088 | CS087 | CS086 | ... | CS003 | CS002 | CS001 |
| | | | DI1 | X | X | X | X | X | X | X |
| | | | DI2 | X | X | X | X | X | X | X |
| | | | DI3 | X | X | X | X | X | X | X |
| H | COM_FLM Input | SEG_END Output | DI0 | CS033 | CS034 | CS035 | ... | CS118 | CS119 | CS120 |
| | | | DI1 | X | X | X | X | X | X | X |
| | | | DI2 | X | X | X | X | X | X | X |
| | | | DI3 | X | X | X | X | X | X | X |

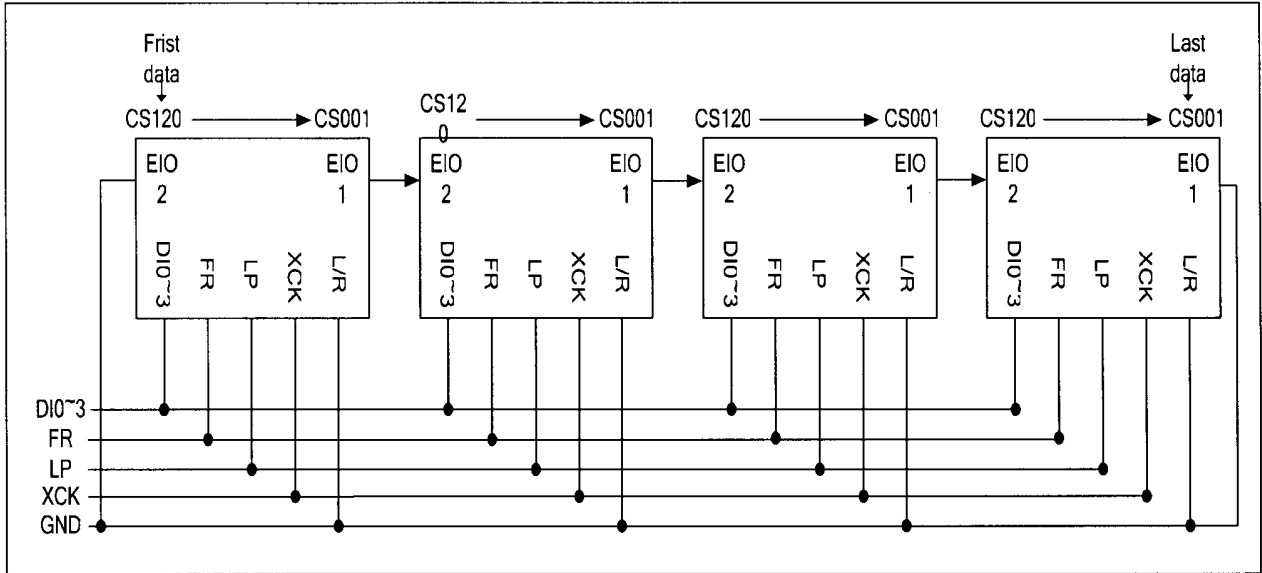
COMMON SIDE OF MIX MODE

| L/R | DATA/TRANSFER/DIRECTION | EIO1 | EIO2 |
|-----|-------------------------|----------------|----------------|
| L | CS120...CS089 | SEG_END/output | Input |
| H | CS001...CS032 | Input | SEG_END/output |

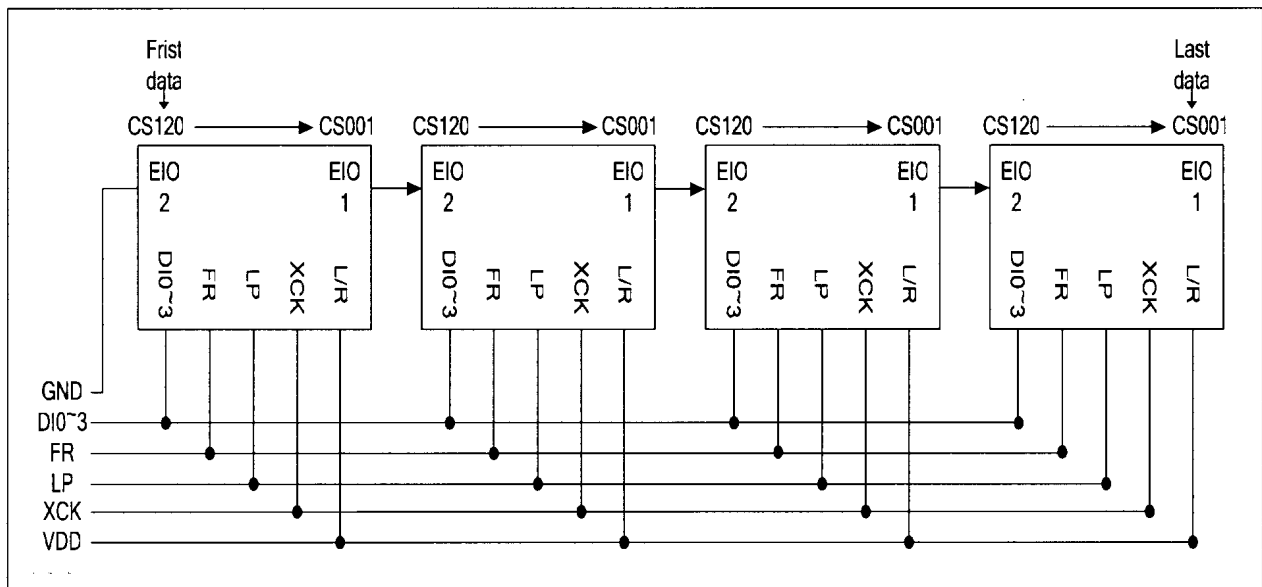


Cascading Two or More LCD Drivers (Segment Mode)

When L/R = 'L'

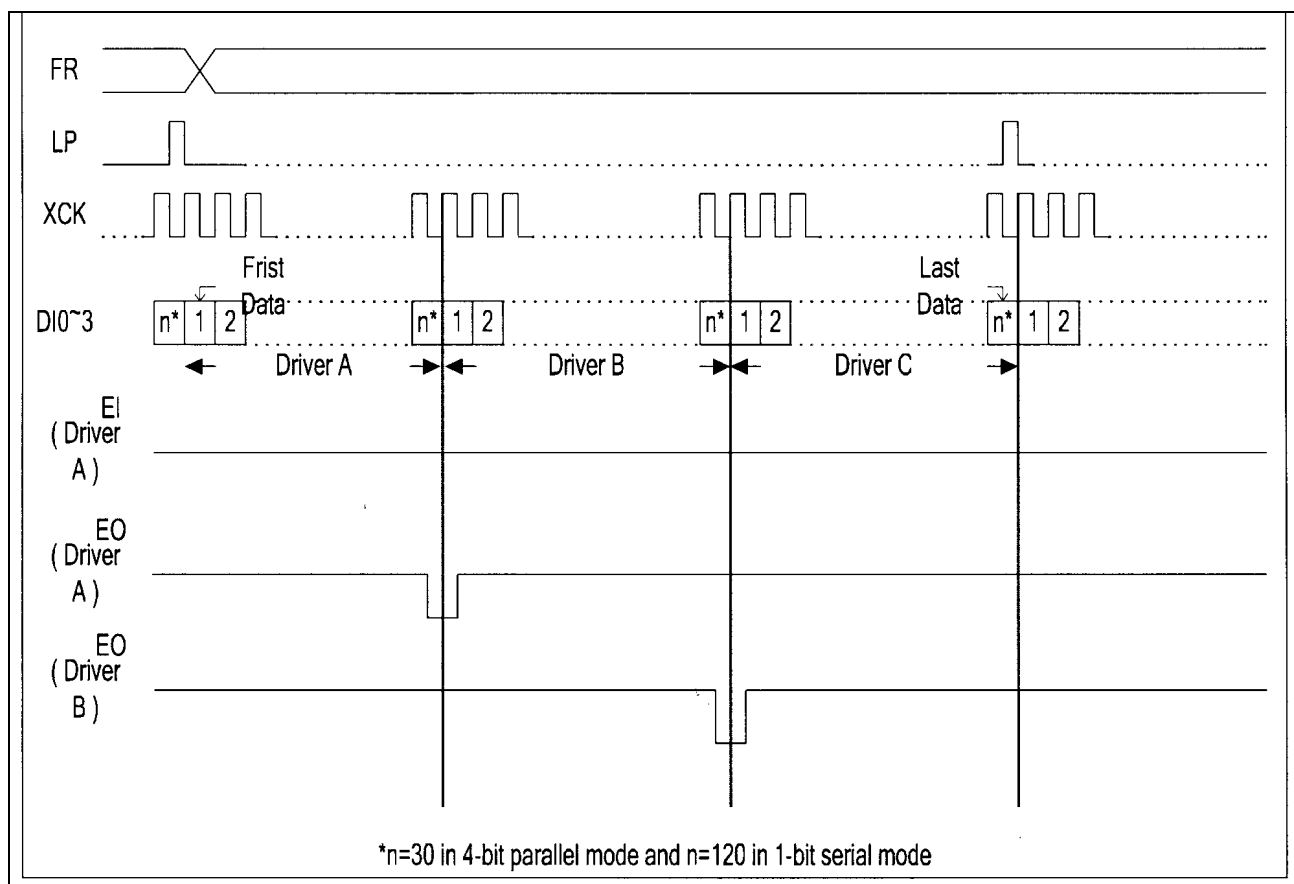


When L/R = 'H'



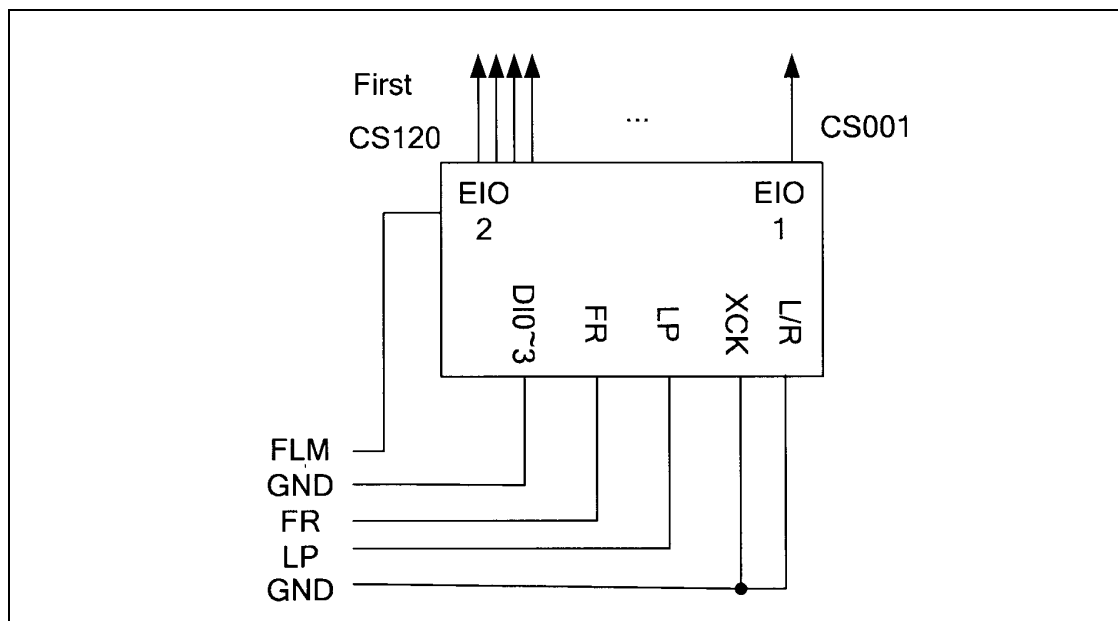


Timing Diagram of Cascaded Three Drivers

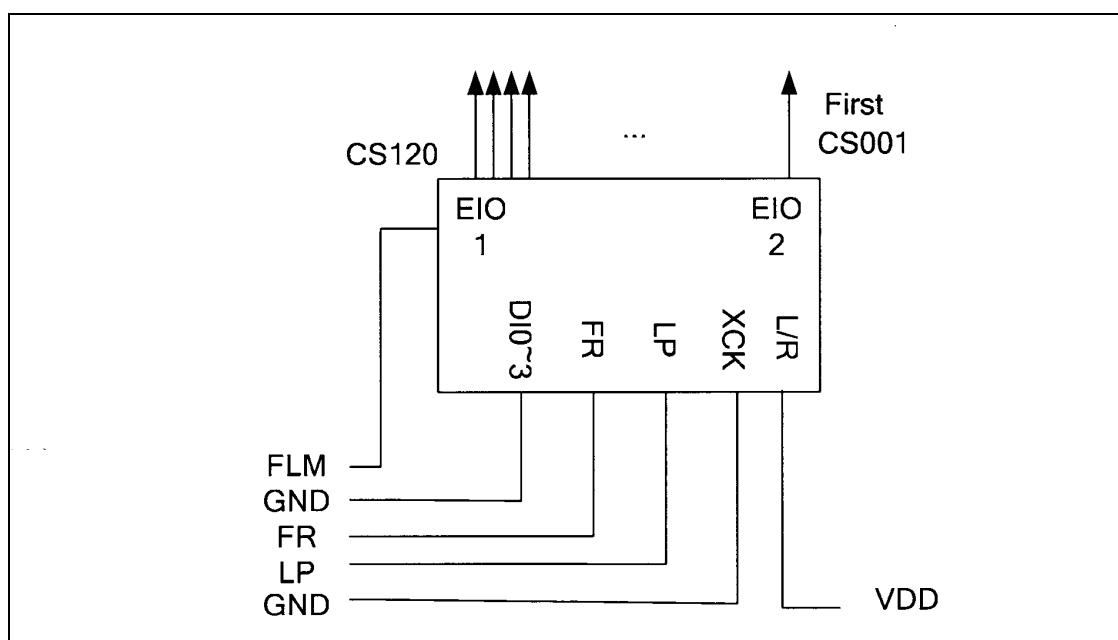


Connection one signal common driver (120 Common)

- When L/R = 'L'



- When L/R = 'H'

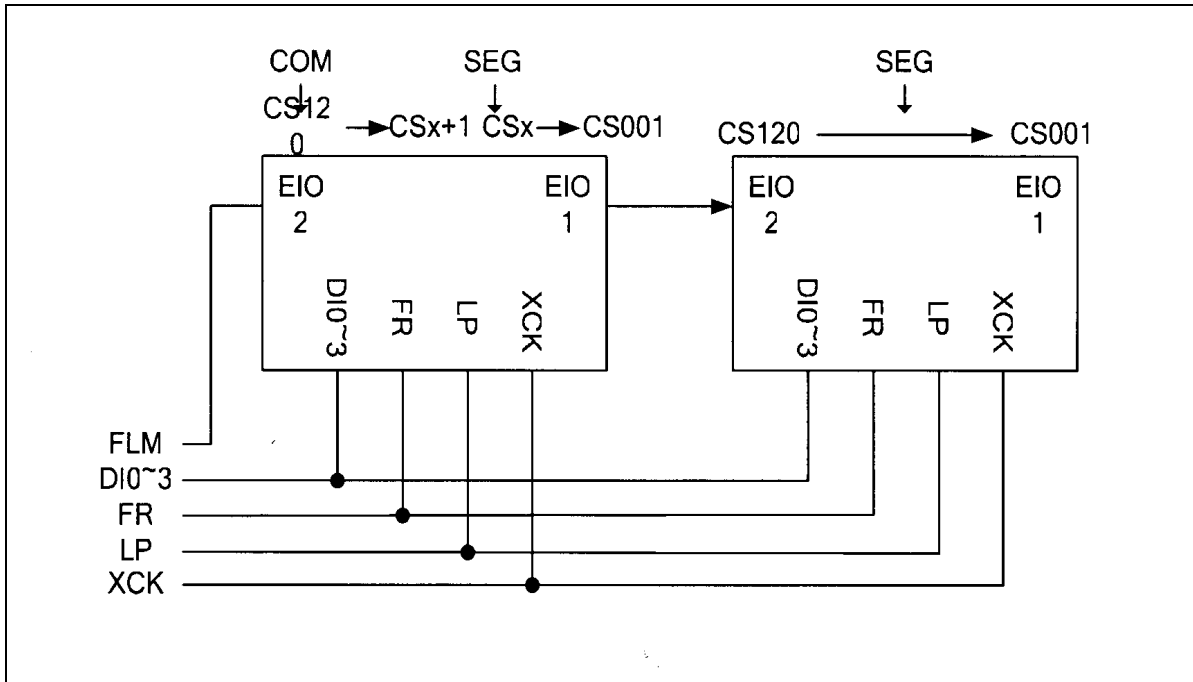




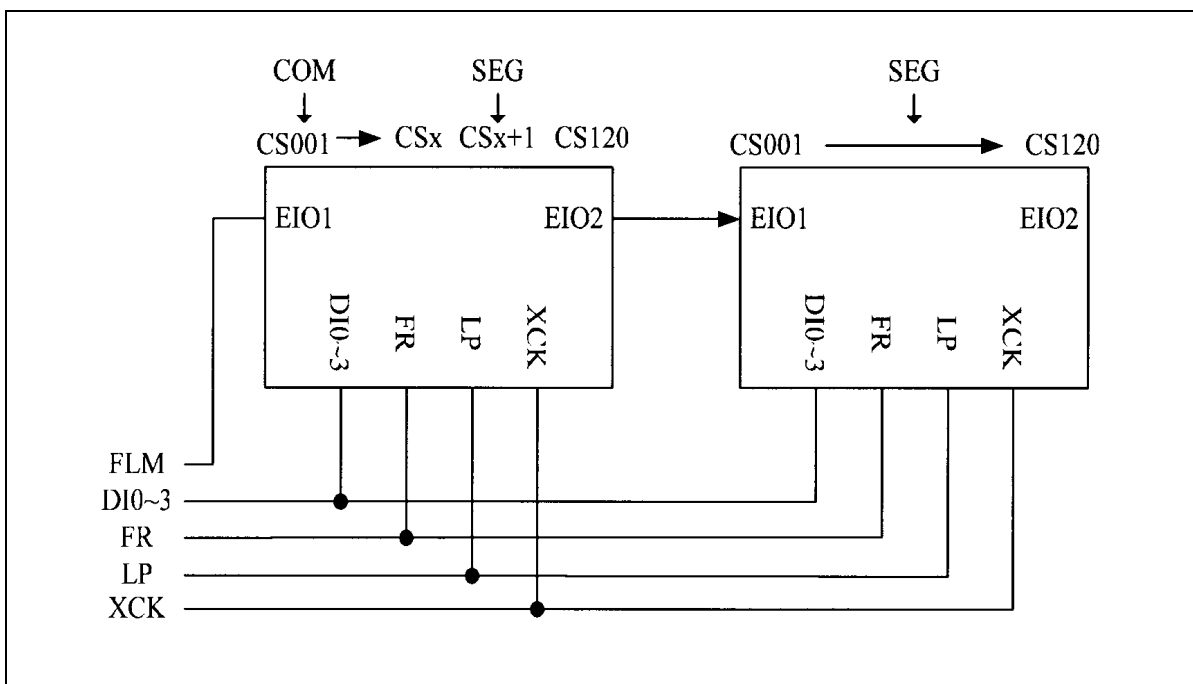
Connection mix mode driver (Common/Segment)

If mix mode is 1/32, 1/48, 1/64, 1/80, 1/96, 1/112 duty mode

- When L/R = 'L'



- When L/R = 'H'



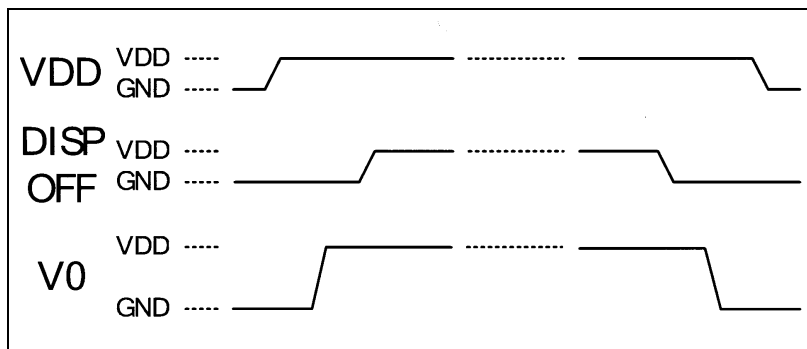


POWER PRECAUTION

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows, when connecting the power supply; connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on DISPOFF function. After that, cancel the DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level GND on DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



THE INTERFACE WITH MCU

This section is description about the data serial interface.

- **Command Serial interface**

In the An6812, instruction transfers are done through a serial data input interface. The timing show illustrated in Figure 1.

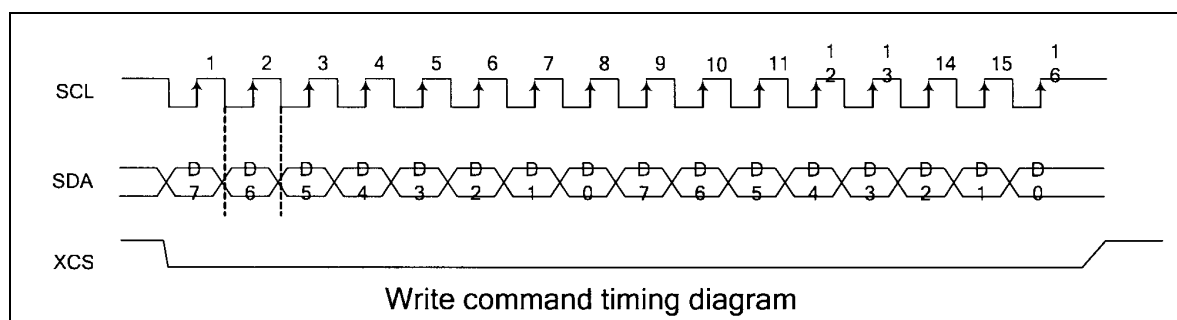


Figure 1. Serial interface timing diagram

THE POWER SUPPLY CIRCUITS

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation, when the mode is in common mode or common/segment mode. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set instruction. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 1 shows the related bits for Power Control Set instruction, and reference combinations.

Table 1. The Control Details of Each Bit of the Power Control Set Command

| D2 | D1 | D0 | Voltage booster | Voltage regulator | Voltage follower | External voltage input | Step-up voltage to VOUT |
|----|----------------|----|-----------------|-------------------|------------------|------------------------|-------------------------|
| 1 | 1 | 1 | ON | ON | ON | VDD | Used |
| 1 | 1 | 0 | ON | ON | OFF | VDD, V1~V4 | Used |
| 1 | 0 | 1 | ON | OFF | ON | VDD, V0 | Used |
| 1 | 0 | 0 | ON | OFF | OFF | VDD, V0~V4 | Used |
| 0 | 1 | 1 | OFF | ON | ON | VDD, VOUT | Open |
| 0 | 0 | 1 | OFF | OFF | ON | VDD, V0=VOUT | OPEN |
| 0 | 1 | 0 | OFF | ON | OFF | VDD, VOUT, V1~V4 | OPEN |
| 0 | 0 ¹ | 0 | OFF | OFF | OFF | VDD, V0=VOUT, V1~V4 | Open |

- **MCU Interface Unused Mode**

When MCU interface is unused the XCS, SCK, and SDA signal can set the related power control with **XRST signal from low go high**, as a power on reset. That is, when XRST from low go high, the power status bits will be latched as D2 is from XCS, D1 from SCK, and D0 from SDA. MCU can use simpler I/O methods to control An6812.



THE STEP-UP VOLTAGE CIRCUITS

Using the step-up voltage circuits equipped within the An6812 chips, it is possible to produce a 2X, 3X, 4X, 5X or 6X step-up of the V_{DD} -GND voltage levels.

- **2X step-up**

Connect capacitor C1 between C1P+ and C1N, and between V_{DD} and V_{OUT} . Leave C2N open, and short C2P, C3P, C4P, C5P and V_{OUT} to produce a voltage level at the V_{OUT} terminal that is twice the voltage V_{DD} and GND. The step up voltage relationships are show in Figure 2

- **3X step-up**

Connect capacitor C1 between C1P+ and C1N, between C2P+ and C2N, between V_{DD} and V_{OUT} , and short between C3P, C4P, C5P and V_{OUT} to produce a voltage level at the V_{OUT} terminal that is 3 times the voltage level between V_{DD} and GND. The step up voltage relationships are show in Figure 2.

- **4X step-up**

Connect capacitor C1 between C1P and C1N, between C2P+ and C2N, between C3P and C1N, and between V_{DD} and V_{OUT} , and short between C4P, C5P and V_{OUT} to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and GND. The step up voltage relationships are show in Figure 2.

- **5X step-up**

Connect capacitor C1 between C1P and C1N, between C2P and C2N, between C3P and C1N, between C4P and C2N, and between V_{DD} and V_{OUT} , and short between C5P and V_{OUT} to produce a voltage level at the V_{OUT} terminal that is 5 times the voltage level between V_{DD} and GND. The step up voltage relationships are show in Figure 2.

- **6X step-up**

Connect capacitor C1 between C1P+ and C1N, between C2P and C2N, between C3P and C1N, between C4P and C2N, between C5P and C1N, and between V_{DD} and V_{OUT} to produce a voltage level at the V_{OUT} terminal that is 6 times the voltage level between V_{DD} and GND. The step up voltage relationships are show in Figure 2.

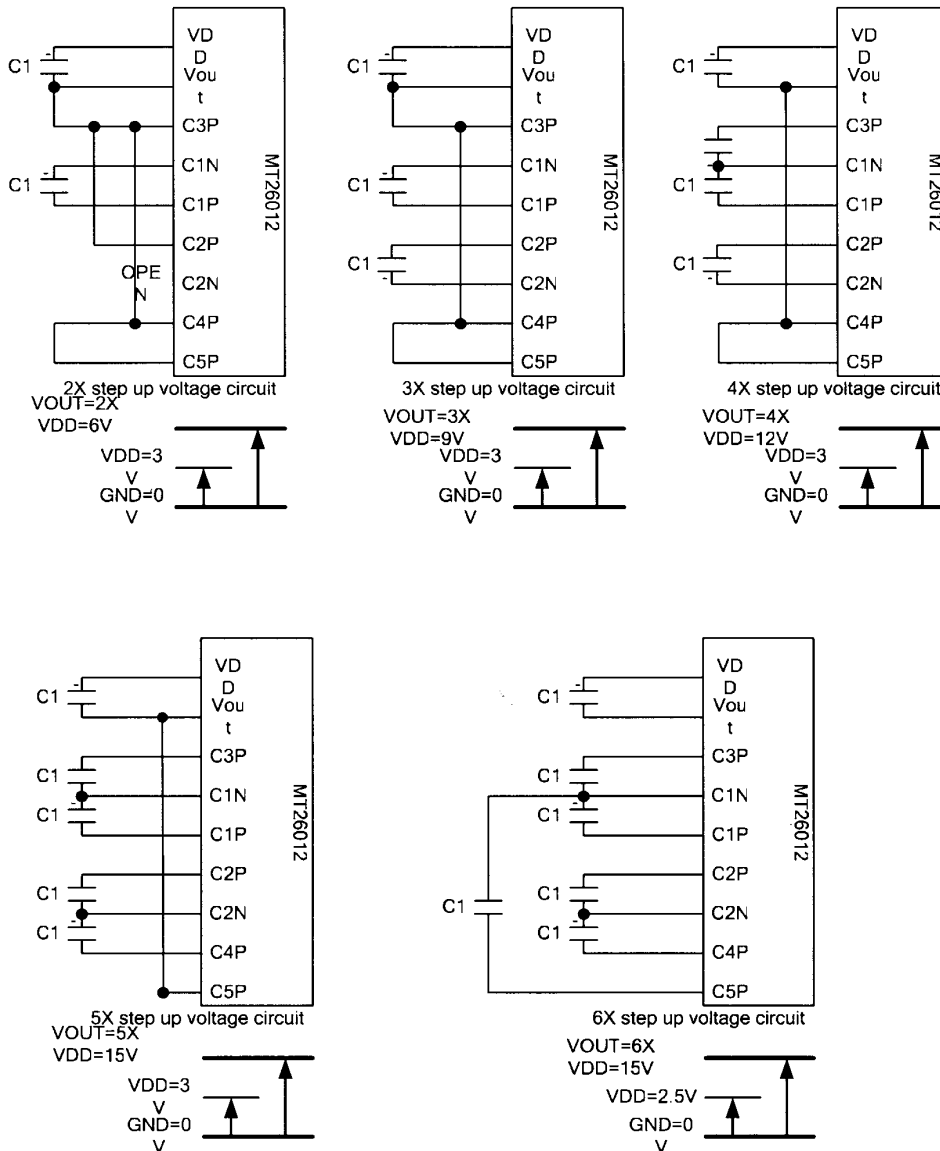


Figure 2. The step up voltage relationships

THE VOLTAGE REGULATOR CIRCUIT

The step-up voltage generated at V_{OUT} will be regulated as the LCD drive voltage V_0 through the voltage regulator circuit. Because the An6812 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. The voltage regulator circuits are shown in Figure 3.

When the V_0 Voltage Regulator internal Resistors Are Used

Through the use of the V_0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V_0 can be controlled by instructions alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V_0 voltage can be calculated using equation A-1 over the range where $|V_0| < |V_{OUT}|$.

$$V_0 = (1+R_b/R_a) \cdot V_{EV} = (1+R_b/R_a) \cdot (1 \cdot /200) \cdot V_{REG}$$

$$[V_{EV} = (1 \cdot /200) \cdot V_{REG}]$$

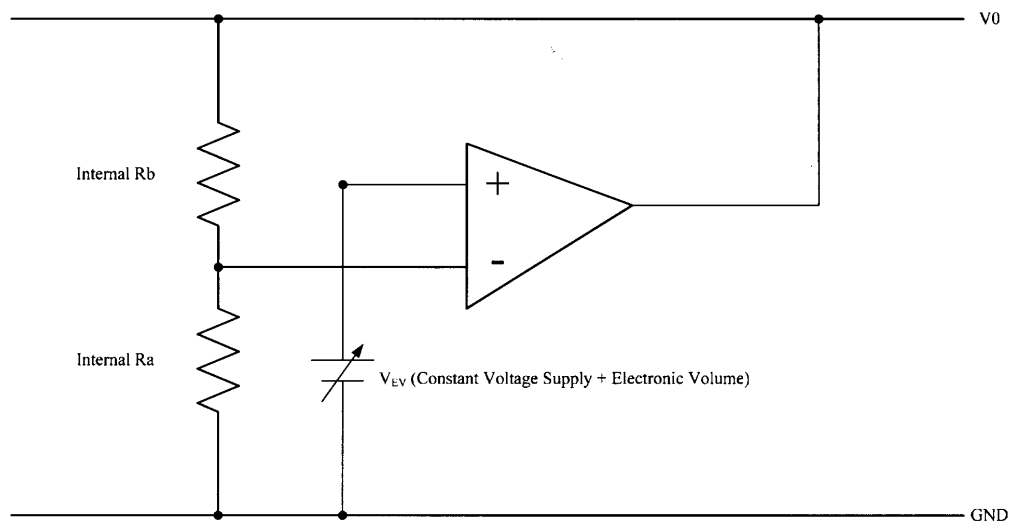


Figure 3. Internal Regulator Circuit



The VREG Voltage Description

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 2

Table 2. The V_{REG} Voltage

| Part no. | Equipment Type | Thermal Gradient | V _{REG} |
|----------|-----------------------|------------------|------------------|
| An6812 | Internal Power Supply | -0.05%/°C | 2.1V |

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 3 shows the value for α depending on the electronic volume register settings.

Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage

regulator internal resistor ratio set command. The Rb/Ra ratio assumes the values shown in Table 4 depending on

the 3-bit data settings in the VDD voltage regulator internal resistor ratio register.

Table 3. α depending on the electronic volume register setting

| D5 | D4 | D3 | D2 | D1 | D0 | α |
|----|----|----|----|----|----|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 63 |
| 0 | 0 | 0 | 0 | 0 | 1 | 62 |
| 0 | 0 | 0 | 0 | 1 | 0 | 61 |
| | | | | | | ⋮ |
| | | | | | | ⋮ |
| 1 | 1 | 1 | 1 | 0 | 1 | 2 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 |

V0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 4. (1+.....) depending on the 3-bit data settings

| HV | Register | | | MT26012 |
|----|----------|----|----|------------------|
| | D2 | D1 | D0 | (1+Rb/Ra) @ 25°C |
| 0 | 0 | 0 | 0 | 5.0 |
| | 0 | 0 | 1 | 5.22 |
| | 0 | 1 | 0 | 5.48 |
| | 0 | 1 | 1 | 5.76 |
| | 1 | 0 | 0 | 6.07 |
| | 1 | 0 | 1 | 6.42 |
| | 1 | 1 | 0 | 6.81 |
| | 1 | 1 | 1 | 7.25 |
| 1 | 0 | 0 | 0 | |
| | 0 | 0 | 1 | |
| | 0 | 1 | 0 | |
| | 0 | 1 | 1 | |
| | 1 | 0 | 0 | |
| | 1 | 0 | 1 | |
| | 1 | 1 | 0 | |
| | 1 | 1 | 1 | |

THE LCD VOLTAGE GENERATOR CIRCUIT

The V_0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1 , V_2 , V_3 , and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1 , V_2 , V_3 , and V_4 to the liquid crystal drive circuit.

Reference Circuit Examples

1. When the voltage booster circuit and V/F circuit are used (External Voltage Regulator)

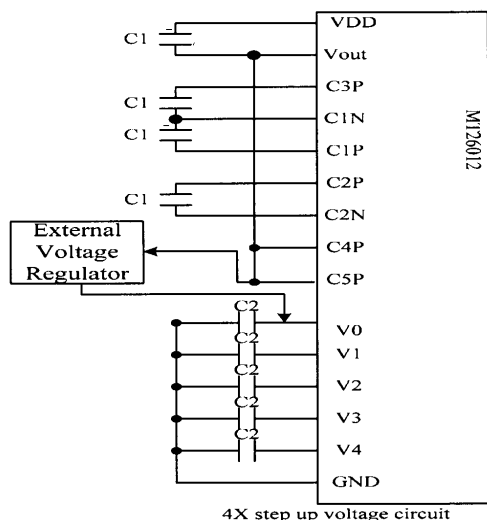


Figure 4. Using External voltage regulator.

2. When used all of the step-up circuit, voltage regulating circuit and V/F circuit.

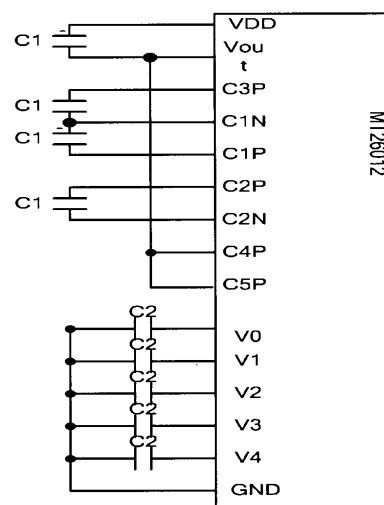


Figure 5. Using internal regulating circuits.

3. When the voltage regulator circuit and V/F circuit alone are used

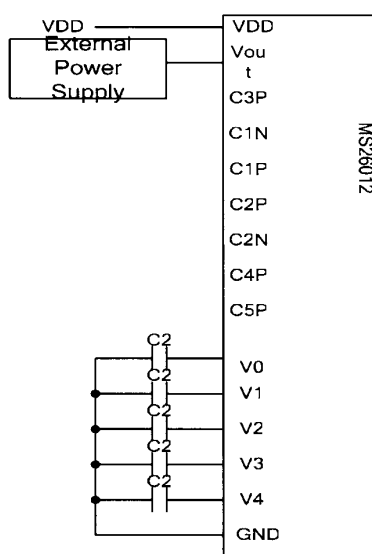


Figure 6. When external supply with internal regulator is used.



4. When the V/F circuit alone is used.

5. When the built-in power is not used.

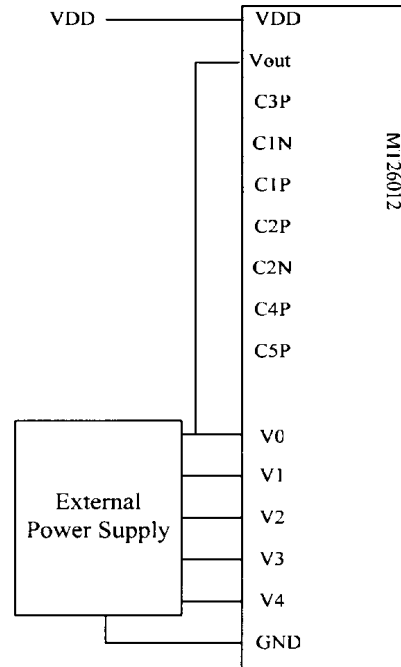
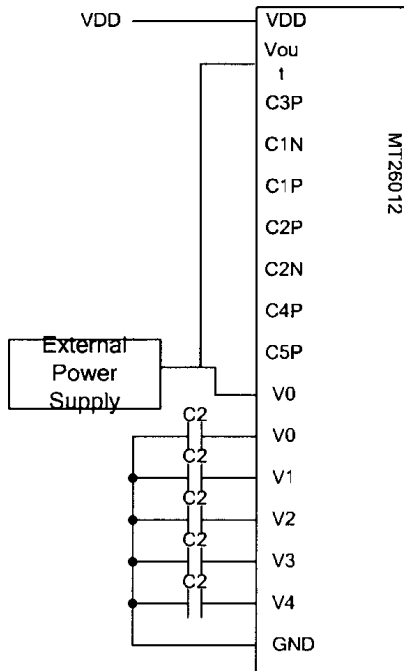
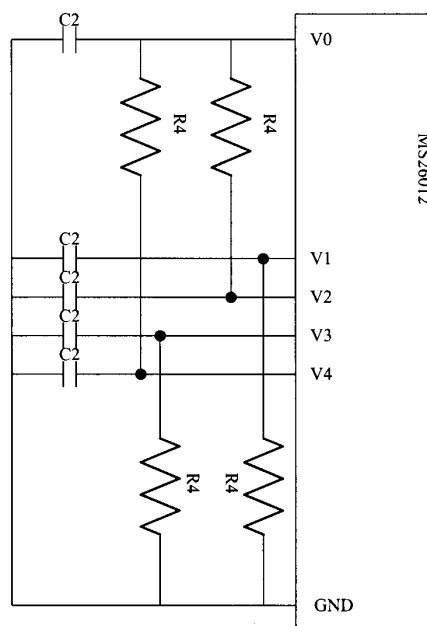


Figure 7. When external supply & regulator is used.

Figure 8. When external supply & V/F are used.

6. When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V1, V2, V3, and V4 which are output from the built-in voltage follower. Examples of shared reference settings When V0 can vary between 7V and 25V.





Reference set value R4: 100KΩ ~ 1MΩ it is recommended to set an optimum resistance value R4 taking the liquid crystal display and the drive waveform.

- *1. Because the V1~4 terminal input impedance is high, use short leads and shielded lines.
- *2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

| Item | Set/value | Units |
|------|-----------|-------|
| C1 | 1.0~4.7 | μF |
| C2 | 0.1~4.7 | μF |

C1 and C2 are determined by the size of the LCD being driven.

- Example of the Process by which to Determine the Settings:
- Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to VOUT from the outside.
- Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V1 to V4). Note that all C2 capacitors must have the same capacitance value.
- Next turn all the power supplies ON and determine C1.

MCU INTERFACE INSTRUCTION TABLE

| Instruction | Code Instruction | | | | | | | | Description |
|-------------------------|------------------|----|-----|-----|-----|---------|---------|---------|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| LCD Bias Set | 0 | 0 | 0 | 0 | FD | BS2 | BS1 | BS0 | FD=0: internal frame direction is normal, FD=1: Internal frame direction is reversed BS2~BS0: when HV=0, set bias from 1/5 to 1/12 when HV=1, set bias from 1/10 to 1/17 |
| Power Control Set | 0 | 0 | 1 | 0 | HV | BS T | RE G | FL W | HV: An6812 is in high voltage mode BST: ON/OFF Voltage booster REG: ON/OFF regulator FLW: ON/OFF voltage follower |
| Internal Resistor Ratio | 0 | 1 | 0 | 0 | X | Rab2 | Rab1 | Rab0 | Select internal resistor ratio (1+Rb/Ra) for V0 voltage level control |
| Electronic Volume Set | 1 | 1 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 | Select Vref reference voltage α |
| Booster Frequency Set | 0 | 1 | 1 | 0 | X | BF2 | BF1 | BF0 | Select Booster frequency |

**MCU INTERFACE INSTRUCTION DESCRIPTION**

An6812 identify the data bus signals by a combination of SDA., SCL signals.

LCD Bias Set

This command selects bias ratio of An6812 at different duty settings.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|-----|-----|-----|
| 0 | 0 | 0 | 0 | FD | BS2 | BS1 | BS0 |

FD: Frame direction control bit

When FD= "1", the internal frame direction and external frame direction are the same. (Normally)

When FD= "0", the internal frame direction and external frame direction are adverse.

BS2~BS0: Bias set from 1/5 to 1/12 at low voltage mode (HV=0) and from 1/10 to 1/17 at high voltage mode (HV=1).

| HV | BS2 | BS1 | BS0 | Bias | V1 | V2 | V3 | V4 |
|----|-----|-----|------|----------|----------|----------|---------|---------|
| 0 | 0 | 0 | 0 | 1/5 | 4/5*V0 | 3/5*V0 | 2/5*V0 | 1/5*V0 |
| | 0 | 0 | 1 | 1/6 | 5/6*V0 | 4/6*V0 | 2/6*V0 | 1/6*V0 |
| | 0 | 1 | 0 | 1/7 | 6/7*V0 | 5/7*V0 | 2/7*V0 | 1/7*V0 |
| | 0 | 1 | 1 | 1/8 | 7/8*V0 | 6/8*V0 | 2/8*V0 | 1/8*V0 |
| | 1 | 0 | 0 | 1/9 | 8/9*V0 | 7/9*V0 | 2/9*V0 | 1/9*V0 |
| | 1 | 0 | 1 | 1/10 | 9/10*V0 | 8/10*V0 | 2/10*V0 | 1/10*V0 |
| | 1 | 1 | 0 | 1/11 | 10/11*V0 | 9/11*V0 | 2/11*V0 | 1/11*V0 |
| 1 | 1 | 1 | 1 | 1/12 | 11/12*V0 | 10/12*V0 | 2/12*V0 | 1/12*V0 |
| | 0 | 0 | 0 | 1/10 | 9/10*V0 | 8/10*V0 | 2/10*V0 | 1/10*V0 |
| | 0 | 0 | 1 | 1/11 | 10/11*V0 | 9/11*V0 | 2/11*V0 | 1/11*V0 |
| | 0 | 1 | 0 | 1/12 | 11/12*V0 | 10/12*V0 | 2/12*V0 | 1/12*V0 |
| | 0 | 1 | 1 | 1/13 | 12/13*V0 | 11/13*V0 | 2/13*V0 | 1/13*V0 |
| | 1 | 0 | 0 | 1/14 | 13/14*V0 | 12/14*V0 | 2/14*V0 | 1/14*V0 |
| | 1 | 0 | 1 | 1/15 | 14/15*V0 | 13/15*V0 | 2/15*V0 | 1/15*V0 |
| | 1 | 1 | 0 | 1/16 | 15/16*V0 | 14/16*V0 | 2/16*V0 | 1/16*V0 |
| 1 | 1 | 1 | 1/17 | 16/17*V0 | 15/17*V0 | 2/17*V0 | 1/17*V0 | |

Power Controller Set

The power Controller Set command is as follows.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|-----|-----|-----|
| 0 | 0 | 0 | 0 | HV | BST | REG | FLW |

HV: Select high voltage mode (HV=1) or low voltage mode (HV=0),

BST=1: Turn ON voltage booster,

BST=0: Turn OFF voltage booster

REG=1: Turn ON voltage regulator

REG=0: Turn OFF Voltage regulator

FLW=1: Turn ON Voltage follower

FLW=0: Turn OFF voltage follower.



Internal Regulator Reference Voltage Resistor Ratio Set

The reference voltage of An6812 voltage regulator has the resistor ratio set as below:

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|------|------|------|
| 0 | 1 | 0 | 0 | X | Rab2 | Rab1 | Rab0 |

The ratio is as the following table:

| HV | Register | | | MT26012 |
|----|----------|------|------|------------------|
| | Rab2 | Rab1 | Rab0 | (1+Rb/Ra) @ 25°C |
| 0 | 0 | 0 | 0 | 5.00 |
| | 0 | 0 | 1 | 5.22 |
| | 0 | 1 | 0 | 5.48 |
| | 0 | 1 | 1 | 5.76 |
| | 1 | 0 | 0 | 6.07 |
| | 1 | 0 | 1 | 6.42 |
| | 1 | 1 | 0 | 6.81 |
| 1 | 1 | 1 | 1 | 7.25 |
| | 0 | 0 | 0 | |
| | 0 | 0 | 1 | |
| | 0 | 1 | 0 | |
| | 0 | 1 | 1 | |
| | 1 | 0 | 0 | |
| | 1 | 0 | 1 | |
| | 1 | 1 | 0 | |
| | 1 | 1 | 1 | |

Electronic volume of Reference Voltage Set

The reference voltage volume α of An6812 voltage regulator has the command set as below:

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |

The set parameter is as follows.

| EV5 | EV4 | EV3 | EV2 | EV1 | EV0 | • |
|-----|-----|-----|-----|-----|-----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 63 |
| 0 | 0 | 0 | 0 | 0 | 1 | 62 |
| 0 | 0 | 0 | 0 | 1 | 0 | 61 |
| | | | | | | : |
| | | | | | | : |
| 1 | 1 | 1 | 1 | 0 | 1 | 2 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 |

Voltage Boost Frequency Set

The voltage booster frequency can be set by the command below:

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|-----|-----|-----|
| 0 | 1 | 1 | 0 | X | BF2 | BF1 | BF0 |



The set frequency (Typical) is as the following table:

| BF2 | BF1 | BF0 | Frequency @ 25°C |
|-----|-----|-----|------------------|
| 0 | 0 | 0 | 1k |
| 0 | 0 | 1 | 2k |
| 0 | 1 | 0 | 3k |
| 0 | 1 | 1 | 4k |
| 1 | 0 | 0 | 5k |
| 1 | 0 | 1 | 6k |
| 1 | 1 | 0 | 7k |
| 1 | 1 | 1 | 8k |

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | APPLICABLE PINS | RATING | UNIT | NOTE |
|---------------------|--------|--|-----------------|------|------|
| Supply voltage (1) | VDD | VDD | -0.3~5.5 | V | 2,3 |
| Supply voltage (2) | V0 | V0 | VDD+20~VDD-0.3 | V | |
| | V1 | V1 | VDD+20~VDD-0.3 | V | |
| | V2 | V2 | VDD+20~VDD-0.3 | V | |
| | V3 | V3 | -0.3~GND+20 | V | |
| | V4 | V4 | -0.3~GND+20 | V | |
| Input voltage | Vin | D14-D10, XCK, F/R, EIO1, EI02, DISPOFF | -0.3 to VDD+0.3 | V | |
| Storage/temperature | TSTG | | -45to+125 | °C | |

NOTES :

1. TA= +25°C
2. The maximum applicable voltage on any pin with respect to GND (0V).

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|-----------------------|--------|-----------------|------|------|-------|------|------|
| Supply voltage (1) | VDD | VDD | +2.4 | | +5.5 | V | 2,3 |
| Supply voltage (2) | V0 | V0 | +5.0 | | +25.0 | V | |
| Operating temperature | TOPR | | -20 | +85 | °C | | |

² The applicable voltage on pin with respect to GND (0V).

³ Ensure that voltages are set such that V0≥V1≥V2≥V3≥V4≥GND.



ELECTRICAL CHARACTERISTICS

DC Characteristics

In the Segment Mode (GND=0V, VDD=+2.5 to 5.5V, V0=+5V to +15V, T_{OPR}=-20~+85°C)

| PARAMENTER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP | MAX. | UNIT | NOTE |
|---|------------------|---------------------------------|--|----------------------|-----|--------------------|------|----------------------|
| Supply Voltage (1) | VDD | | VDD | 2.4 | | 5.5 | V | |
| Supply Voltage (2) | V0 | | V0 | 5.0 | | 25 | V | V _{OUT} ≥V0 |
| Supply Voltage (3) | Vout | | Vout | 5.0 | | 25 | V | V _{OUT} ≥V0 |
| Input "Low" voltage | V _{IL} | | DI ₃ -DI ₀ , XCK, L/P, L/R, FR, EIO ₁ , EIO ₂ , DISPOFF | | | 0.2V _{DD} | V | |
| Input "High" voltage | V _{IH} | | | 0.8V _{DD} | | | V | |
| Output "Low" voltage | V _{OL} | I _{OL} =+0.4mA | EIO ₁ , EIO ₂ | | | +0.4 | V | |
| Output "High" voltage | V _{OH} | I _{OH} =-0.4mA | | V _{DD} -0.4 | | | V | |
| Input leakage current | I _{LIL} | V _I =GND | DI ₃ -DI ₀ , XCK, L/P, L/R, FR, EIO ₁ , EIO ₂ , DISPOFF | | | -10 | μA | |
| | I _{LIH} | V _I =V _{DD} | | | | +10 | μA | |
| Output resistance | R _{ON} | $\frac{ V_{ON} =0.5V}{V_0=30V}$ | CS ₀ -CS ₉₅ | | 1.0 | 1.5 | k | |
| Standby current | I _{STB} | | GND | | | 5 | μA | 5 |
| Supply current (1) (Non -selection) | I _{DD1} | | V _{DD} | | | 2.0 | mA | 6 |
| Supply current (2) (selection) | I _{DD2} | | V _{DD} | | | 7.0 | mA | 7 |
| Supply current (3) | I ₀ | | V ₀ ,V _{DD} | | | 0.9 | mA | 8 |

⁵ V_{DD} = +3.0V, V0 = +15.0V, booster OFF.

⁶ V_{DD} = +3.0V, V0 = +15.0V, f_{xck} = 8MHz, no-load, EI = VDD. The input data is turned over by data taking clock (4-bit parallel input mode).

⁷ V_{DD} = +3.0V, V0 = +15.0V, f_{xck} = 8MHz, no-load, EI = GND. The input data is turned over by data taking clock (4-bit parallel input mode).

⁸ V_{DD} = +3.0V, V0 = +15.0V, f_{xck} = 8MHz, no-load, EI = GND. The input data is turned over by data taking clock (4-bit parallel input mode).



In the Common Mode & Common/Segment Mixed Mode (GND=0V, VDD=+2.5 to 5.5V, V0=+15V to +25V, T_{OPR}=-20~+85 °C)

| PARAMENTER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP | MAX. | UNIT | NOTE |
|--|------------------|---------------------------------|---|----------------------|-----|--------------------|------|----------------------|
| Supply Voltage (1) | VDD | | VDD | 2.4 | | 5.5 | V | |
| Supply Voltage (2) | V0 | | V0 | 5.0 | | 25 | V | V _{out} ≥V0 |
| Supply Voltage (3) | V _{out} | | V _{out} | 5.0 | | 25 | V | V _{out} ≥V0 |
| Input "Low" voltage | V _{IL} | | DI ₃ -DI ₀ , XCK, FR, EIO ₁ , EIO ₂ , DISPOFF | | | 0.2V _{DD} | V | |
| Input "High" voltage | V _{IH} | | | 0.8V _{DD} | | | V | |
| Output "Low" voltage | V _{OL} | I _{OL} =+0.4mA | EIO ₁ , EIO ₂ | | | +0.4 | V | |
| Output "High" voltage | V _{OH} | I _{OH} =-0.4mA | | V _{DD} -0.4 | | | V | |
| Input leakage current | I _{LIL} | V _i =GND | DI ₃ -DI ₀ , FR, P/S, EIO ₁ , EIO ₂ , DISPOFF | | | -10 | μA | |
| | I _{LIH} | V _i =V _{DD} | | | | +10 | μA | |
| Input pull-down current | L _{PD} | | XCK EIO ₁ , EIO ₂ | | | | μA | |
| Output resistance | R _{ON} | V _{ON} =0.5V | CS ₀ -CS ₉₅ | | 1.0 | 1.5 | k | |
| | | V ₀ =16V | | | | | | |
| Standby current | I _{SPD} | | GND | | | 5 | μA | 9 |
| Supply current (1) | I _{DD} | | V _{DD} | | | 80 | μA | 10 |
| Supply current (2) | I ₀ | | V _{DD} | | | 130 | μA | 10 |
| Output Voltage with 4x voltage booster | V _{O1} | V _{DD} =5.0V | V _{out} | 18.0 | | | V | 11 |
| Output Voltage with 6x voltage booster | V _{O2} | V _{DD} =3.0V | V _{out} | 15.0 | | | V | 11 |

⁹ V_{DD} = +5.0V, V0 = +25.0V, V_i = GND.

¹⁰ V_{DD} = +5.0V, V0 = +25.0V, f_{LP} = 19.2MHz, f_{FR} = 80Hz 1/120 duty operation, no-load.

¹¹ External Capacitors C1 in Figure 2 are all 3.3μF, and ILOAD=450 μA, 25°C, voltage follower ON.

**DC Offset of V0~V4**

The following table shows the offset voltages of V0~V4 while driving LCD. Test condition is as follows:

- a) $\alpha = 0$, $(1+R_b/R_a)=7.25$, regulator ON,
- b) External Power Supply to $V_{out}=18.0V$.
- c) 1/10 bias,
- d) External Capacitors: $1\mu F$ as Figure 6.
- e) Temperature = $-20\sim 75^{\circ}C$.

| | No Load | | Max Load | | Max Load (Reverse Electric Current) | | Unit |
|-----------------|---------|------|----------|------|-------------------------------------|-----|------|
| | Min | Max | Min | Max | Min | Max | V |
| V0 | 14.7 | 15.7 | 14.6 | 15.6 | - | - | V |
| $\Delta V1$ | -100 | 90 | -110 | 75 | -110 | 110 | mV |
| $\Delta V2$ | -65 | 65 | -50 | 75 | -110 | 110 | mV |
| $\Delta V3$ | -70 | 70 | -85 | 50 | -110 | 110 | mV |
| $\Delta V4$ | -55 | 50 | -45 | 65 | -110 | 110 | mV |
| X^{12} | -220 | 190 | -225 | 145 | - | - | mV |
| Y^{13} | -120 | 130 | -170 | 85 | - | - | mV |
| ΔV^{14} | -210 | 190 | -300 | 12- | - | - | mV |

The Load conditions is as follows,

| | No Load | Max Load | Max Load | Unit |
|----|---------|----------|----------|---------|
| I0 | 0 | -300 | - | μA |
| I1 | 0 | -50 | 50 | μA |
| I2 | 0 | 200 | -100 | μA |
| I3 | 0 | -200 | 100 | μA |
| I4 | 0 | 50 | -50 | μA |

¹² $X=(V1-V2)-(V0-V1)$, which means ON/Off duty, non-lighting, first half frame LCD Driving DC offset.

¹³ $Y=(V3-V4)-(V4-GND)$, which means ON/OFF duty, non-lighting, second frame LCD Driving DC offset.

¹⁴ VOM balance $\Delta V=X+Y$, which means the DC offset that will act on LCD panel constantly.

**AC Characteristics**In the Segment Mode 1 (GND=0V, VDD=2.5~3.6V, V0=6.0~16.0V, T_{OPR}=-20~85°C)

| PARAMENTER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|--|-------------|------|------|------|------|------|
| Shift clock period | t _{WCK} | tR ,tF≤11ns | 125 | | | ns | 15 |
| Shift clock "H" pulse width | t _{WCKH} | | 50 | | | ns | |
| Shift clock "L" pulse width | t _{WCKL} | | 50 | | | ns | |
| Data setup time | t _{DS} | | 30 | | | ns | |
| Data hold time | t _{DH} | | 40 | | | ns | |
| Latch pulse "H" pulse width | t _{WLPH} | | 50 | | | ns | |
| Shift clock rise to latch pulse rise time | t _{LD} | | 0 | | | ns | |
| Shift clock fall to latch pulse fall time | t _{SL} | | 51 | | | ns | |
| Latch pulse rise to shirt clock rise time | t _{LS} | | 51 | | | ns | |
| Latch pulse fall to shift clock fall time | t _{LH} | | 51 | | | ns | |
| Enable setup time | t _S | | 36 | | | ns | |
| Input signal rise time | t _R | | | | 50 | ns | 16 |
| Input signal fall time | t _F | | | | 50 | ns | 16 |
| DISPOFF removal time | t _{SD} | | 100 | | | ns | |
| DISPOFF "L" pulse width | t _{WDL} | | 1.2 | | | us | |
| Output delay time (1) | t _D | CL=15pF | | | 78 | ns | |
| Output delay time (2) | t _{PD1} , t _{PD2} | CL=15pF | | | 1.2 | us | |
| Output delay time (3) | t _{PD3} | CL=15pF | | | 1.2 | us | |

¹⁵ Takes the cascade connection into consideration.

¹⁶ (TWCK-TWCKH-TWCKL)/2 is maximum in the case of high speed operation.

**In the Segment Mode 2 (GND=0V, VDD=4.5~5.5V, V0=6.0~16.0V, T_{OPR}=-20~85°C)**

| PARAMENTER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|-------------------------------------|-------------------------------------|------|------|------|------|------|
| Shift clock period | t _{WCK} | t _R t _F ≤10ns | 66 | | | ns | 17 |
| Shift clock "H" pulse Width | t _{WCKH} | | 23 | | | ns | |
| Shift clock "L" pulse width | t _{WCKL} | | 23 | | | ns | |
| Data setup time | t _{DS} | | 15 | | | ns | |
| Data hold time | t _{DH} | | 23 | | | ns | |
| Latch pulse "H" pulse width | t _{WLPH} | | 30 | | | ns | |
| Shift clock rise to latch pulse rise time | t _{LD} | | 0 | | | ns | |
| Shift clock fall to latch pulse fall time | t _{SL} | | 50 | | | ns | |
| Latch pulse rise to shift clock rise time | t _{LS} | | 30 | | | ns | |
| Latch pulse fall to shift clock fall time | t _{LH} | | 30 | | | ns | |
| Enable setup time | t _S | | 15 | | | ns | |
| Input signal rise time | t _R | | | | 50 | ns | 18 |
| Input signal fall time | t _F | | | | 50 | ns | 18 |
| DISPOFF removal time | t _{SD} | | 100 | | | ns | |
| DISPOFF "L" pulse width | t _{WDL} | | 1.2 | | | μs | |
| Output delay time (1) | t _D | CL=15PF | | | 41 | ns | |
| Output delay time (2) | t _{PD1} , t _{PD2} | CL=15PF | | | 1.2 | μs | |
| Output delay time (3) | t _{PD3} | CL=15PF | | | 1.2 | μs | |

¹⁷ Takes the cascade connection into consideration.

¹⁸ $(T_{WCK} - T_{WCKH} - T_{WCKL})/2$ is maximum in the case of high speed operation.

**In the Segment Mode 3 (GND=0V, VDD=3.0V~3.6V, V0=6.0~16.0V, T_{OPR}=-20~85⁰C)**

| PARAMENTER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|------------------------------------|--------------|------|------|------|------|------|
| Shift clock period | t _{WCK} | tR, tF≤10 ns | 82 | | | ns | 19 |
| Shift clock "H" pulse width | t _{WCKH} | | 28 | | | ns | |
| Shift clock "L" pulse width | T _{wckl} | | 28 | | | ns | |
| Data setup time | t _{DS} | | 20 | | | ns | |
| Data hold time | t _{DH} | | 23 | | | ns | |
| Latch pulse "H" pulse width | t _{WLPH} | | 30 | | | ns | |
| Shift clock rise to latch pulse rise time | t _{LD} | | 0 | | | ns | |
| Shift clock fall to latch pulse fall time | t _{SL} | | 51 | | | ns | |
| Latch pulse rise to shirt clock rise time | t _{LS} | | 30 | | | ns | |
| Latch pulse fall to shift clock fall time | t _{LH} | | 30 | | | ns | |
| Enable setup time | t _S | | 15 | | | ns | |
| Input signal rise time | t _R | | | | 50 | ns | 20 |
| Input signal fall time | t _F | | | | 50 | ns | 20 |
| DISPOFF removal time | t _{SD} | | 100 | | | ns | |
| DISPOFF "L" pulse width | t _{WDL} | | 1.2 | | | μs | |
| Output delay time (1) | t _D | CL=15PF | | | 57 | ns | |
| Output delay time (2) | t _{PD1} ,t _{PD2} | CL=15PF | | | 1.2 | μs | |
| Output delay time (3) | t _{PD3} | CL=15PF | | | 1.2 | μs | |

¹⁹ Takes the cascade connection into consideration.

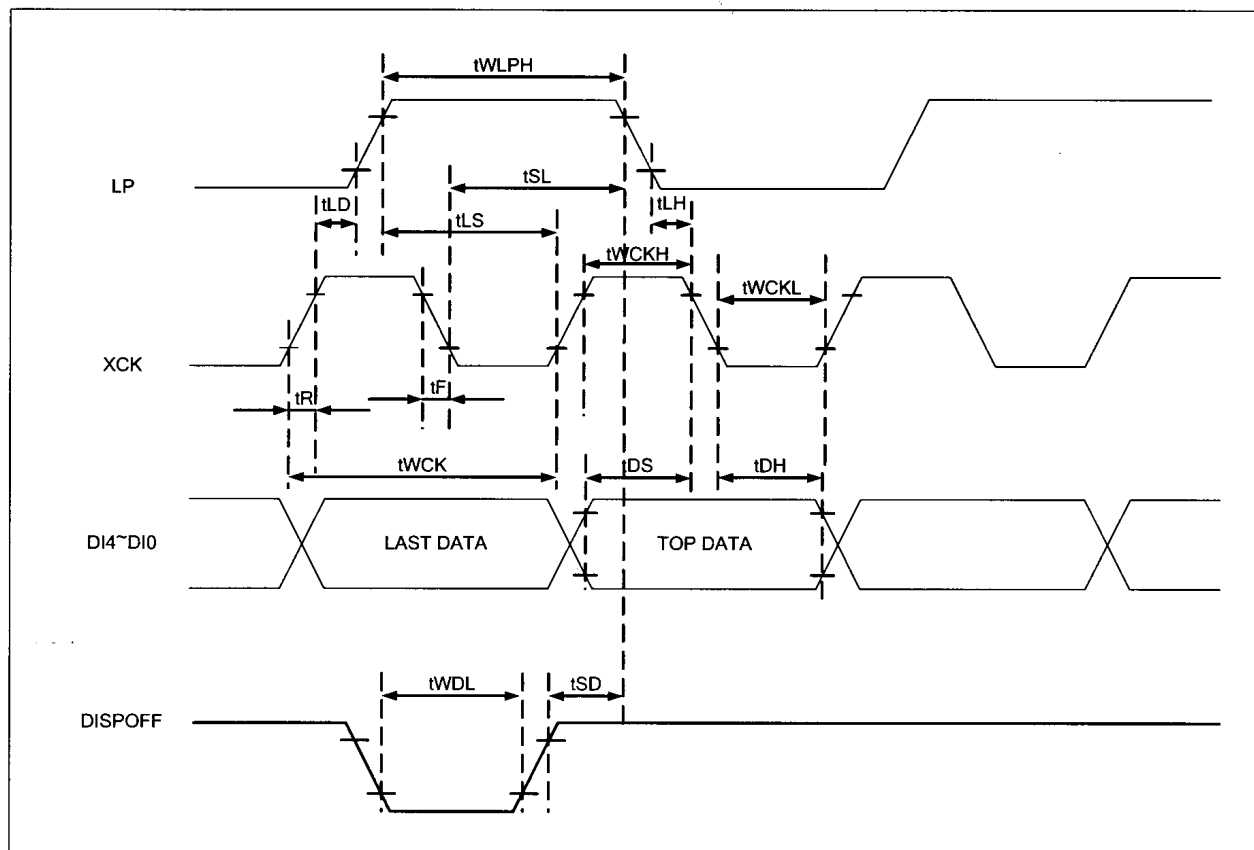
²⁰ (TWCK-TWCKH-TWCKL)/2 is maximum in the case of high speed operation.

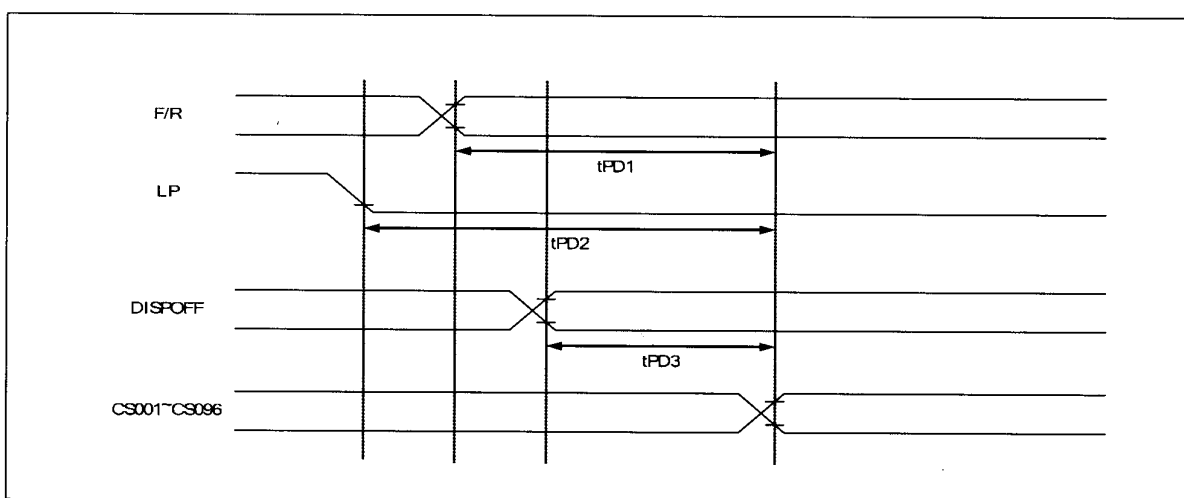
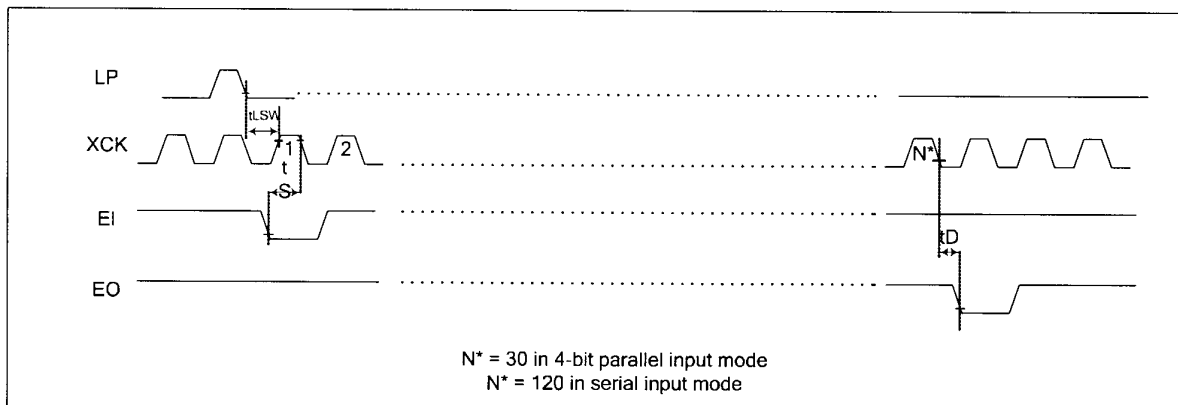


In the Common Mode (GND=0V, VDD=2.5V~5.5V, V0=5.0~16.0V, TOPR=-20~85°C)

| PARAMENTER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------------|--------------------|-----------------|------|------|------|------|
| Shift clock period | t_{WLP} | $t_R, t_F 20ns$ | 250 | | | ns |
| Shift clock "H" pulse width | t_{WLPH} | VDD=5±0.5V | 15 | | | ns |
| | | VDD=2.5~4.5V | 30 | | | |
| Data setup time | t_{SU} | | 30 | | | ns |
| Data hold time | t_H | | 50 | | | ns |
| Input signal rise time | t_R | | | | 50 | ns |
| Input signal fall time | t_F | | | | 50 | ns |
| DISPOFF removal time | t_{SD} | | 100 | | | ns |
| DISPOFF "L" pulse width | t_{WDL} | | 1.2 | | | us |
| Output delay time (1) | t_{DL} | CL=10pF | | | 200 | ns |
| Output delay time (2) | t_{PD1}, t_{PD2} | CL=10pF | | | 1.2 | us |
| Output delay time (3) | t_{PD3} | CL=10pF | | | 1.2 | us |

TIMING CHART OF SEGMENT MODE



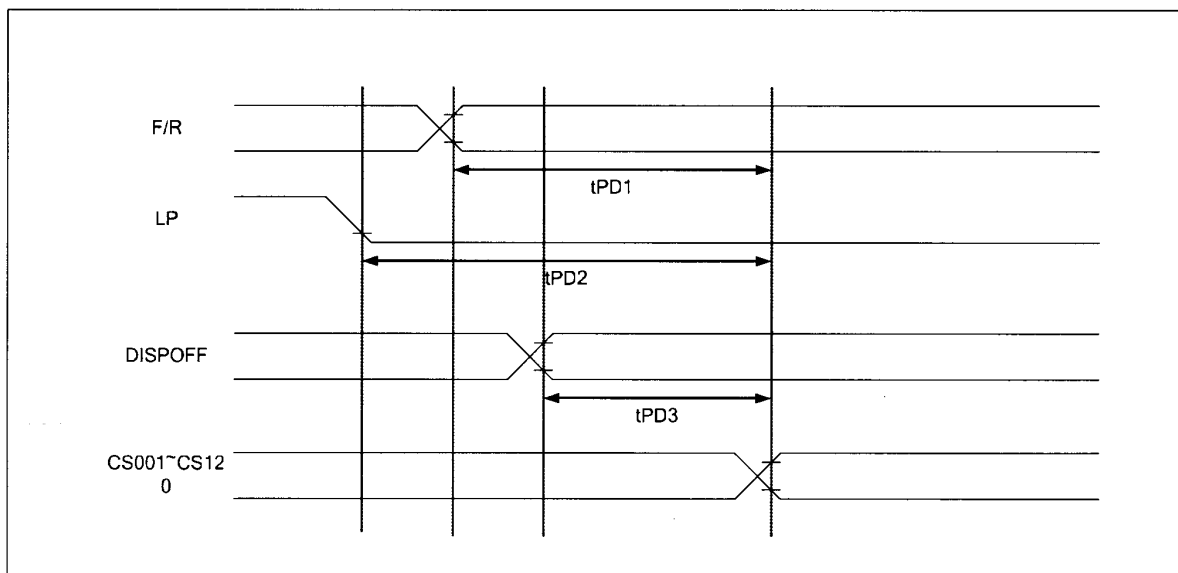
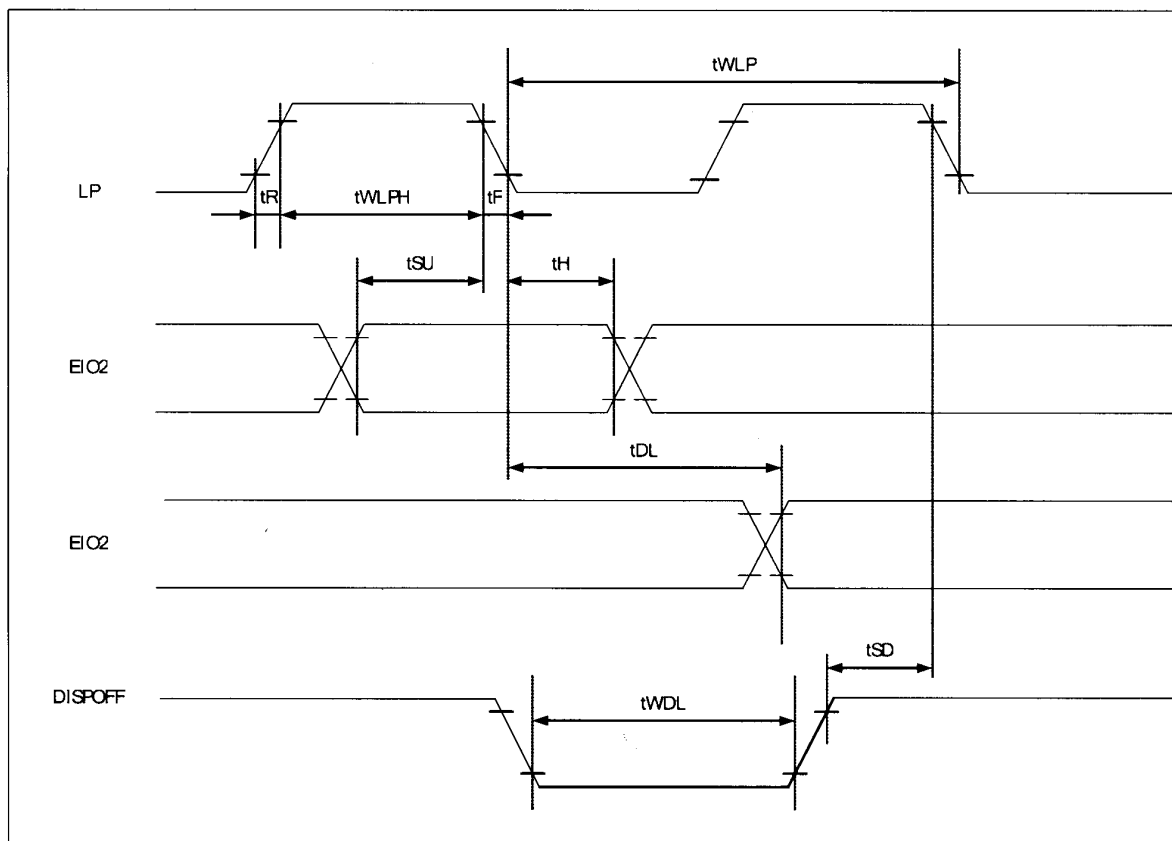


In the Common Mode 2 (GND=0V, VDD=2.5V~3.6V, V0=5.0~16.0V, TOPR=-20~85°C)

| PARAMENTER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------------|--------------------|-----------------|------|------|------|------|
| Shift clock period | t_{WLP} | $t_r, t_f 20ns$ | 250 | | | ns |
| Shift clock "H" pulse width | t_{WLPH} | VDD=5±0.5V | 15 | | | ns |
| | | VDD=2.5~4.5V | 30 | | | ns |
| Data setup time | t_{SU} | | 30 | | | ns |
| Data hold time | t_H | | 50 | | | ns |
| Input signal rise time | t_R | | | | 50 | ns |
| Input signal fall time | t_F | | | | 50 | ns |
| DISPOFF removal time | t_{SD} | | 100 | | | ns |
| DISPOFF "L" pulse width | t_{WDL} | | 1.2 | | | us |
| Output delay time (1) | t_{DL} | CL=15pF | | | 200 | ns |
| Output delay time (2) | t_{PD1}, t_{PD2} | CL=15pF | | | 1.2 | us |
| Output delay time (3) | t_{PD3} | CL=15pF | | | 1.2 | us |

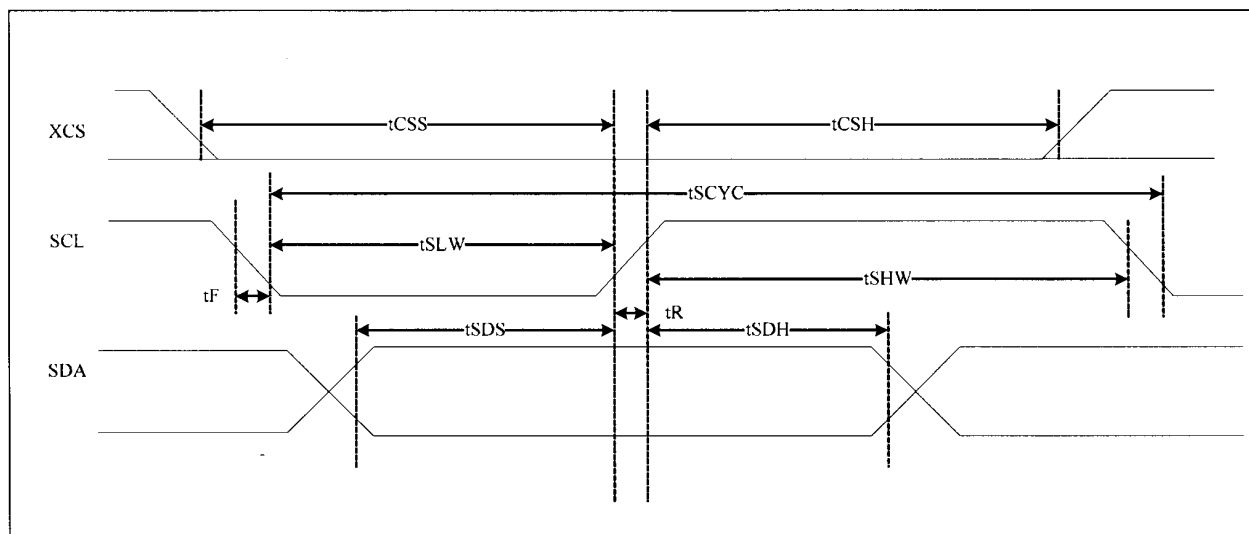


TIMING CHART OF COMMON MODE





TIMING CHART OF MCU INTERFACE

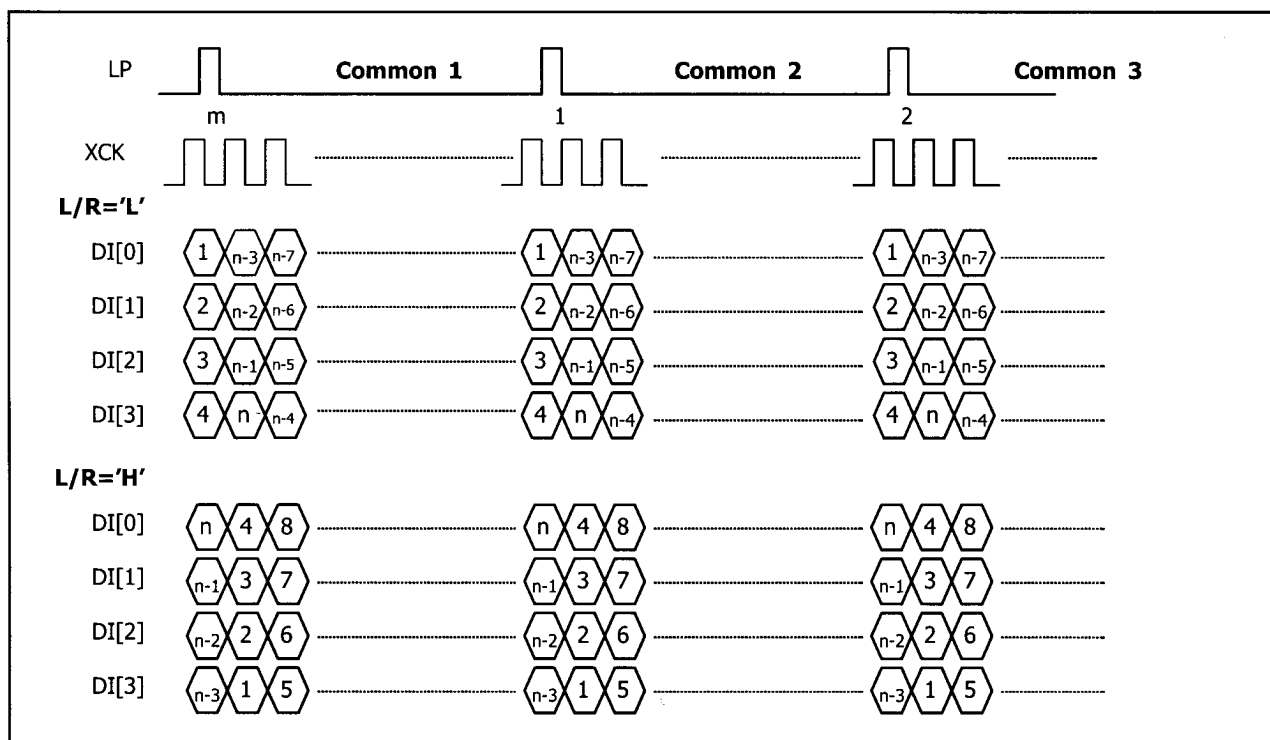


AC Characteristics of MCU Interface (VDD=2.5~5.5V, -20~85°C)

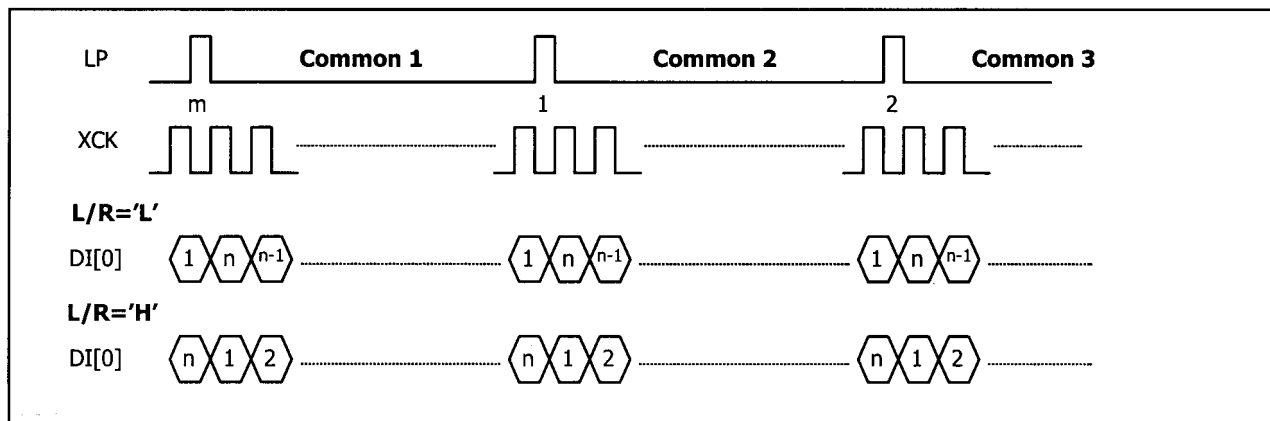
| PARAMENTER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------|--------|-----------------------------|------|------|------|------|
| Serial Clock Period | TSCYC | $t_R, t_F \leq 10\text{ns}$ | 100 | | | ns |
| SCL "H" Pulse Width | TSHW | | 50 | | | |
| SCL "L" Pulse Width | TSLW | | 50 | | | |
| Data Setup time | TSDS | | 30 | | | |
| Data hold time | TSDH | | 20 | | | |
| XCS- SCL time | TCSS | | 30 | | | |
| XCS- SCL time | TCHH | | 60 | | | |



DATA LATCH AND DISPLAY DATA FOR 4-BIT PARALLEL MODE

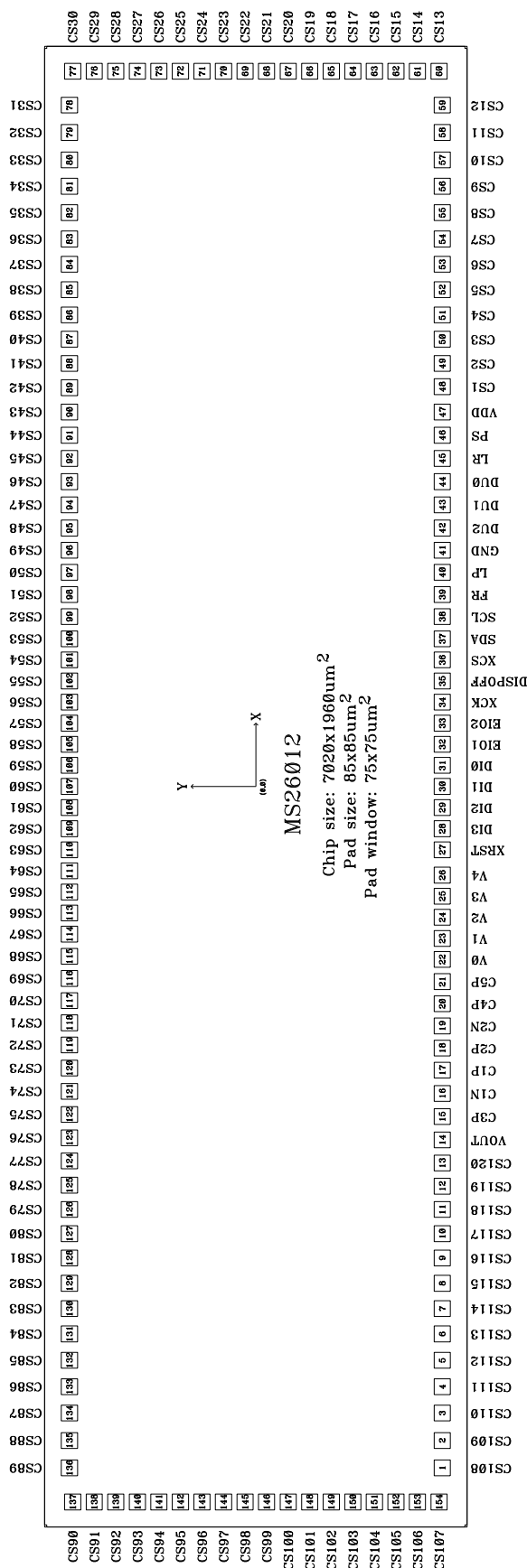


DATA LATCH AND DISPLAY DATA FOR 1-BIT SERIAL MODE





PAD DIAGRAM





PAD LOCATION

| N0 | NAME | COORDINATES | | PAD | NAME | COORDINATES | | N0 | NAME | COORDINATES | | PAD | NAME | COORDINATES | |
|-----|---------|-------------|---------|-----|------|-------------|---|-----|------|-------------|--------|-----|------|-------------|---|
| | | X | Y | | | X | Y | | | X | Y | | | X | Y |
| 1 | CS108 | -3230.00 | -865.00 | | | | | 79 | CS82 | 3100.00 | 865.00 | | | | |
| 2 | CS109 | -3100.00 | -865.00 | | | | | 80 | CS83 | 2970.00 | 865.00 | | | | |
| 3 | CS110 | -2970.00 | -865.00 | | | | | 81 | CS84 | 2845.00 | 865.00 | | | | |
| 4 | CS111 | -2845.00 | -865.00 | | | | | 82 | CS85 | 2720.00 | 865.00 | | | | |
| 5 | CS112 | -2720.00 | -865.00 | | | | | 83 | CS86 | 2595.00 | 865.00 | | | | |
| 6 | CS113 | -2595.00 | -865.00 | | | | | 84 | CS87 | 2475.00 | 865.00 | | | | |
| 7 | CS114 | -2475.00 | -865.00 | | | | | 85 | CS88 | 2355.00 | 865.00 | | | | |
| 8 | CS115 | -2355.00 | -865.00 | | | | | 86 | CS89 | 2235.00 | 865.00 | | | | |
| 9 | CS116 | -2235.00 | -865.00 | | | | | 87 | CS90 | 2120.00 | 865.00 | | | | |
| 10 | CS117 | -2120.00 | -865.00 | | | | | 88 | CS91 | 2005.00 | 865.00 | | | | |
| 11 | CS118 | -2005.00 | -865.00 | | | | | 89 | CS92 | 1890.00 | 865.00 | | | | |
| 12 | CS119 | -1890.00 | -865.00 | | | | | 90 | CS93 | 1775.00 | 865.00 | | | | |
| 13 | CS120 | -1775.00 | -865.00 | | | | | 91 | CS94 | 1665.00 | 865.00 | | | | |
| 14 | VOUT | -1675.00 | -865.00 | | | | | 92 | CS95 | 1555.00 | 865.00 | | | | |
| 15 | C3P | -1565.00 | -865.00 | | | | | 93 | CS96 | 1445.00 | 865.00 | | | | |
| 16 | C1N | -1455.00 | -865.00 | | | | | 94 | CS97 | 1335.00 | 865.00 | | | | |
| 17 | C1P | -1345.00 | -865.00 | | | | | 95 | CS98 | 1225.00 | 865.00 | | | | |
| 18 | C2P | -1240.00 | -865.00 | | | | | 96 | CS99 | 1120.00 | 865.00 | | | | |
| 19 | C2N | -1135.00 | -865.00 | | | | | 97 | CS00 | 1015.00 | 865.00 | | | | |
| 20 | C4P | -1030.00 | -865.00 | | | | | 98 | CS01 | 910.00 | 865.00 | | | | |
| 21 | C5P | -925.00 | -865.00 | | | | | 99 | CS02 | 805.00 | 865.00 | | | | |
| 22 | V0 | -820.00 | -865.00 | | | | | 100 | CS03 | 700.00 | 865.00 | | | | |
| 23 | V1 | -720.00 | -865.00 | | | | | 101 | CS04 | 600.00 | 865.00 | | | | |
| 24 | V2 | -620.00 | -865.00 | | | | | 102 | CS05 | 500.00 | 865.00 | | | | |
| 25 | V3 | -520.00 | -865.00 | | | | | 103 | CS06 | 400.00 | 865.00 | | | | |
| 26 | V4 | -420.00 | -865.00 | | | | | 104 | CS07 | 300.00 | 865.00 | | | | |
| 27 | XRST | -300.00 | -865.00 | | | | | 105 | CS08 | 200.00 | 865.00 | | | | |
| 28 | D13 | -200.00 | -865.00 | | | | | 106 | CS09 | 100.00 | 865.00 | | | | |
| 29 | D12 | -100.00 | -865.00 | | | | | 107 | CS60 | 0.00 | 865.00 | | | | |
| 30 | D11 | 0.00 | -865.00 | | | | | 108 | CS61 | -100.00 | 865.00 | | | | |
| 31 | D10 | 100.00 | -865.00 | | | | | 109 | CS62 | -200.00 | 865.00 | | | | |
| 32 | E101 | 200.00 | -865.00 | | | | | 110 | CS63 | -300.00 | 865.00 | | | | |
| 33 | E102 | 300.00 | -865.00 | | | | | 111 | CS64 | -400.00 | 865.00 | | | | |
| 34 | XCK | 400.00 | -865.00 | | | | | 112 | CS65 | -500.00 | 865.00 | | | | |
| 35 | DISPOFF | 500.00 | -865.00 | | | | | 113 | CS66 | -600.00 | 865.00 | | | | |
| 36 | XCS | 600.00 | -865.00 | | | | | 114 | CS67 | -700.00 | 865.00 | | | | |
| 37 | SDA | 700.00 | -865.00 | | | | | 115 | CS68 | -805.00 | 865.00 | | | | |
| 38 | SCL | 805.00 | -865.00 | | | | | 116 | CS69 | -910.00 | 865.00 | | | | |
| 39 | FR | 910.00 | -865.00 | | | | | 117 | CS70 | -1015.00 | 865.00 | | | | |
| 118 | CS71 | -1120.00 | 865.00 | | | | | 118 | CS82 | 3100.00 | 865.00 | | | | |
| 119 | CS72 | -1225.00 | 865.00 | | | | | 119 | CS83 | 2970.00 | 865.00 | | | | |
| 120 | CS73 | -1335.00 | 865.00 | | | | | 120 | CS84 | 2845.00 | 865.00 | | | | |
| 121 | CS74 | -1445.00 | 865.00 | | | | | 121 | CS85 | 2720.00 | 865.00 | | | | |
| 122 | CS75 | -1555.00 | 865.00 | | | | | 122 | CS86 | 2595.00 | 865.00 | | | | |
| 123 | CS76 | -1665.00 | 865.00 | | | | | 123 | CS87 | 2475.00 | 865.00 | | | | |
| 124 | CS77 | -1775.00 | 865.00 | | | | | 124 | CS88 | 2355.00 | 865.00 | | | | |
| 125 | CS78 | -1890.00 | 865.00 | | | | | 125 | CS89 | 2235.00 | 865.00 | | | | |
| 126 | CS79 | -2005.00 | 865.00 | | | | | 126 | CS90 | 2120.00 | 865.00 | | | | |
| 127 | CS80 | -2120.00 | 865.00 | | | | | 127 | CS91 | 2005.00 | 865.00 | | | | |
| 128 | CS81 | -2235.00 | 865.00 | | | | | 128 | CS92 | 1890.00 | 865.00 | | | | |
| 129 | CS82 | -2355.00 | 865.00 | | | | | 129 | CS93 | 1775.00 | 865.00 | | | | |
| 130 | CS83 | -2475.00 | 865.00 | | | | | 130 | CS94 | 1665.00 | 865.00 | | | | |
| 131 | CS84 | -2595.00 | 865.00 | | | | | 131 | CS95 | 1555.00 | 865.00 | | | | |
| 132 | CS85 | -2720.00 | 865.00 | | | | | 132 | CS96 | 1445.00 | 865.00 | | | | |
| 133 | CS86 | -2845.00 | 865.00 | | | | | 133 | CS97 | 1335.00 | 865.00 | | | | |
| 134 | CS87 | -2970.00 | 865.00 | | | | | 134 | CS98 | 1225.00 | 865.00 | | | | |
| 135 | CS88 | -3100.00 | 865.00 | | | | | 135 | CS99 | 1120.00 | 865.00 | | | | |
| 136 | CS89 | -3230.00 | 865.00 | | | | | 136 | CS00 | 1015.00 | 865.00 | | | | |
| 137 | CS90 | -3391.50 | 850.00 | | | | | 137 | CS01 | 910.00 | 865.00 | | | | |
| 138 | CS91 | -3391.50 | 750.00 | | | | | 138 | CS02 | 805.00 | 865.00 | | | | |
| 139 | CS92 | -3391.50 | 650.00 | | | | | 139 | CS03 | 700.00 | 865.00 | | | | |
| 140 | CS93 | -3391.50 | 550.00 | | | | | 140 | CS04 | 600.00 | 865.00 | | | | |
| 141 | CS94 | -3391.50 | 450.00 | | | | | 141 | CS05 | 500.00 | 865.00 | | | | |
| 142 | CS95 | -3391.50 | 350.00 | | | | | 142 | CS06 | 400.00 | 865.00 | | | | |
| 143 | CS96 | -3391.50 | 250.00 | | | | | 143 | CS07 | 300.00 | 865.00 | | | | |
| 144 | CS97 | -3391.50 | 150.00 | | | | | 144 | CS08 | 200.00 | 865.00 | | | | |
| 145 | CS98 | -3391.50 | 50.00 | | | | | 145 | CS09 | 100.00 | 865.00 | | | | |
| 146 | CS99 | -3391.50 | -50.00 | | | | | 146 | CS60 | 0.00 | 865.00 | | | | |
| 147 | CS100 | -3391.50 | -150.00 | | | | | 147 | CS61 | -100.00 | 865.00 | | | | |
| 148 | CS101 | -3391.50 | -250.00 | | | | | 148 | CS62 | -200.00 | 865.00 | | | | |
| 149 | CS102 | -3391.50 | -350.00 | | | | | 149 | CS63 | -300.00 | 865.00 | | | | |
| 150 | CS103 | -3391.50 | -450.00 | | | | | 150 | CS64 | -400.00 | 865.00 | | | | |
| 151 | CS104 | -3391.50 | -550.00 | | | | | 151 | CS65 | -500.00 | 865.00 | | | | |
| 152 | CS105 | -3391.50 | -650.00 | | | | | 152 | CS66 | -600.00 | 865.00 | | | | |
| 153 | CS106 | -3391.50 | -750.00 | | | | | 153 | CS67 | -700.00 | 865.00 | | | | |
| 154 | CS107 | -3391.50 | -850.00 | | | | | 154 | CS68 | -805.00 | 865.00 | | | | |