An5530 – FDX
128-bit Read-only
IDIC for RF Identification

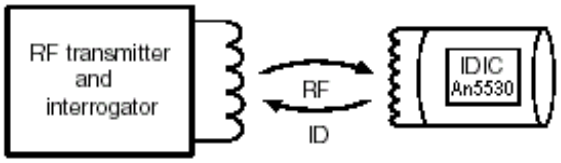
Features

- **Low-power, Low-voltage CMOS**
- **Rectifier, Voltage Limiter, Clock Extraction On-chip (No Battery)**
- **Small Size**
- **Factory Electrically Programmable ROM**
- **Operating Temperature Range -40°C to +125°C**
- **Radio Frequency (RF): 100 kHz to 450 kHz**
- **Transmission options**

– **Code Length: 128 bits**
– **Bitrate [bit/s]: RF/32**
– **Modulation: DBP (differential bi-phase encoding)**

- **FDX-B Compatible Coding Possible (ISO 11784/ ISO 11785)**
- **On-chip resonanse capacitor 250 pF ± 5%**

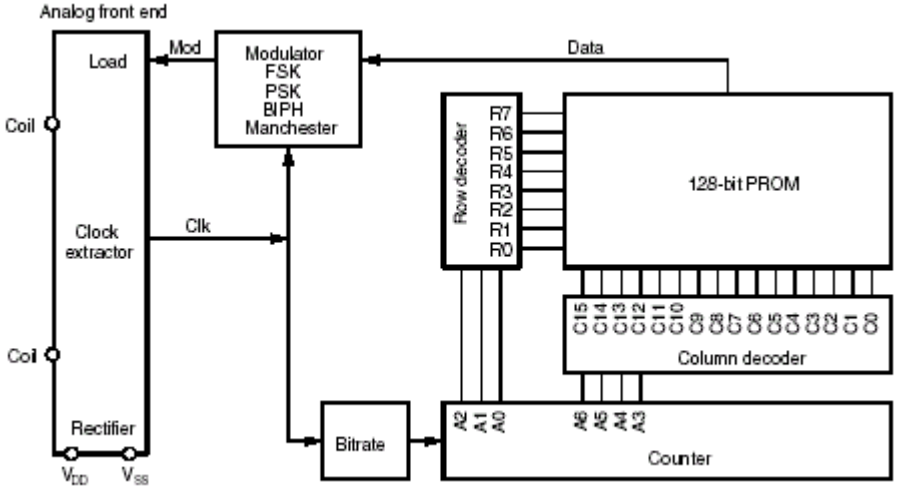
Figure 1. Application



Description

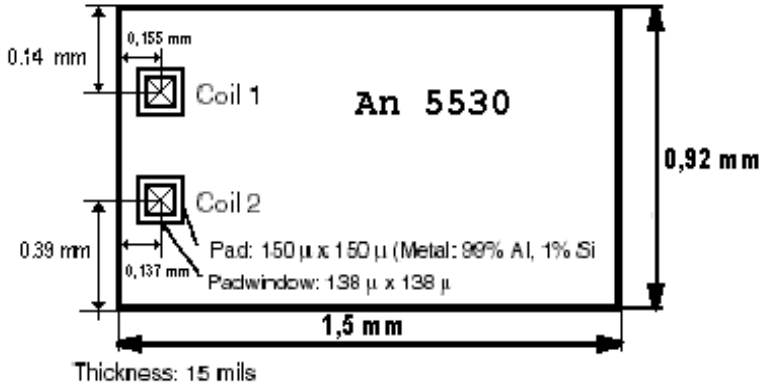
The An5530 is part of a closed coupled identification system. It receives power from an RF transmitter which is coupled inductively to the IDIC.. The frequency is typically 100 kHz to 450 kHz. Receiving RF, the IDIC. responds with a data stream by damping the incoming RF via an internal load. This damping-in-turn can be detected by the interrogator. The identifying data are stored in a 128-bit PROM on the An5530, realized as an array of electrically-programmable fuses. The logic block diagram for the An5530 is shown in figure 2. The data are output bit-serially as a code of length 128 bits. The chips are factory-programmed with a unique code.

Figure 2. Block Diagram



Chip Dimensions

Figure 3. Chip Size



Name	Pad Window	Function
Coil1	138 × 138 µm^2	1st coil pad
Coil2	138 × 138 µm^2	2nd coil pad

Functional Description

Read Operation After power up, once the An5530 has detected the incoming RF field, the IC continuously
transmits the identification code as long as the RF signal is applied. The transition from the last bit to bit 1 of the next sequence occurs without interruption. Data is transmitted by damping the incoming RF signal by an internal load. These load changes are detected by the reader station.
Different kinds of modulation and bitrates are optionally available.

Rectifier For internal power supply, an on-chip Grates bridge rectifier is used which consists of four poly-Si diodes. A Zener diode, which protects the circuit against overvoltage on the coil inputs, and a smoothing capacitor for the internal supply are also provided.

Damping Load Incoming RF will be damped by the power consumption of the IC itself and by an
internal load, which is controlled by the modulator. The loads are p-channel transistors connected between V_{DD} and the coil inputs.
The IDIC includes mask options for the load circuit: single-side, double-side and alternate-side modulation.

Timing Diagram for Modulation Options

5 Abbreviations

AM	amplitude modulation
BCC	block control character
CRC	cyclic redundancy check
DBP	differential bi-phase encoding
FDX	full duplex
FSK	frequency shift keying
HDX	half duplex
LSB	least significant bits
MSB	most significant bits
NRZ	non-return to zero encoding
PSK	phase shift keying
RFID	radio-frequency identification

6 Requirements

The system shall be defined in such a way that the FDX and HDX transponders can be read by one transceiver. Annex A describes the method that can be used to enhance the functionality of this transceiver to read certain installed base transponders which are not compatible with the FDX and HDX transponders described in this clause.

A stationary transceiver shall activate transponders using an activation field with an activation frequency of (134,2 ± 13,42 x 10^{-3}) kHz. The activation period shall be 50 ms. If an FDX signal is received during activation but is not validated, the activation period shall be extended until be identification telegram is validated, but not longer than 100 ms. Consecutively, there shall be a pause in the activation signal. If an HDX signal is received the pause shall last for 20 ms. If no HDX signal is detected within 3 ms after a 3 dB decay of the activation field, activation shall be resumed. For synchronization reasons, each tenth activation cycle shall have a fixed pattern of 50 ms activation and 20 ms pause (see annex C).

A mobile transceiver shall be able to detect the presence of additional active transceivers through the reception of activation signals. If no activation signal is detected within 30 ms, the mobile transceiver is out of reach of other active transceivers and shall use the activation protocol defined above for a stationary transceiver. If the mobile transceiver does detect an activation signal it shall wait for the rising edge of the next activation signal and shall activate during a fixed period of 50 ms.

The identification code shall be in accordance with ISO 11784. The identification code, the CRC error detection bits (see annex B) and the trailer shall be transmitted starting with the LSB and ending with the MSB.

In view of future enhancements, for example multi-page transponders incorporating sensors and/or writable memory, the identification telegram shall terminate in 24 trailer bits in which, for instance, information from sensors or the contents of trailing pages may be stored. If the flag for additional data blocks, which is specified in ISO 11784, is binary 0 the value of most of the trailer bits is unspecified. The value of the trailer bits for additional data blocks which have a flag equal to binary 1 will be defined by a future International Standard.

NOTES

1 Since errors in the trailer will not be detected by the error detection protocol of the identification telegram, it is not necessary to read these bits in order to correctly detect the identification code.

2 In most countries the use of transceivers as described in this International Standard is subject to regulations. Type approval from the national regulatory agencies may be required before they can be operated or traded in these countries.

6.1 Full duplex system

An FDX transponder receiving the activation field shall transmit its code during the activation period. The FDX transponder uses a modified DBP encoded sub-carrier which is amplitude modulated upon the radio frequency

carrier. Because the slope of a low-high transition is not infinitely steep, every low-high transition is advanced in time to a maximum of eight cycles to obtain optimal performance (see figure 1). The transponder shall send its message back using the frequency bands 129,0 kHz to 133,2 kHz and 135,2 kHz to 139,4 kHz. The duration of one bit is 32 activation field cycles. This corresponds to a bit rate of 4 194 bit/s.

NOTE — The basic frequency of the sub-carrier, containing the phase encoded data signal, is not influenced by the advancement in time of the low-high transition and remains 4 194 Hz (binary 1:180° phase shift; binary 0: no phase shift).

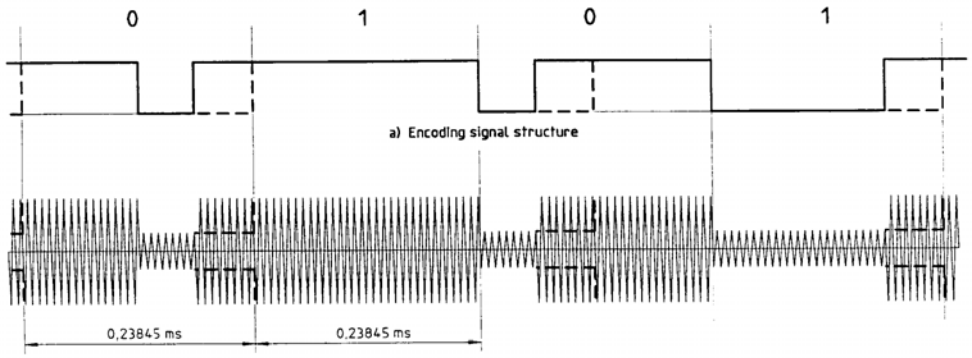


Figure 1 — Signal structures of the FDX identification telegram

The structure of the FDX identification telegram (see figure 2) is as follows:

— a header of 11 bits (00000000001) used to identify the start of the identification telegram;
— a 64-bit identification code transmitted in eight blocks of 8 bits;
— two blocks of 8 bits containing the 16 CRC error detection bits;
— three blocks of 8 bits containing the 24 trailer bits.

The error detection code is calculated solely over the identification code. Each block of 8 bits is trailed by a control bit with the value binary 1 to prevent the appearance of the header in the rest of the identification telegram.

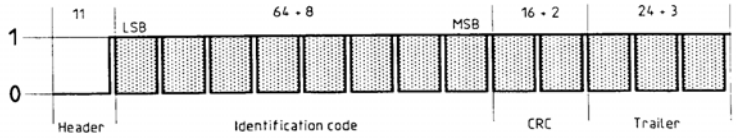


Figure 2 — Structure of the FDX identification telegram

Parameters	Symbol	Value	Unit
Maximum current into Coil1 and Coil2	I_{coil}	10	mA
Maximum power dissipation (dice)	P_{tot}	100	mW (1)
Maximum ambient air temperature with voltage applied	T_{amb}	-40 to +125	°C
Storage temperature	T_{stg}	-65 to +200	°C

Absolute Maximum Ratings

Note: 1. Free-air condition. Time of application: 1 s
Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. Functional operation of the device at these conditions is not implied.

Electrical Characteristics

T_{amb} = 25°C, reference terminal is V_{DD}, operating voltage V_{DD} - V_{SS} = 3 V DC, unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
1	Operating voltage	Condition for logic test	V_{SS}	-1.5		-5.0	V
2	Operating temperature		T_{amb}	-40		125	°C
3	Input frequency (RF)		f_{CLK}	100		450	kHz
4	Operating current	f_{CLK} = 125 kHz, V_{SS} = -2 V	I_{CC}		3 (1)		mA
5	Clamp voltage	I = 4 mA	V_{CL}	6.7		10	V

Note: 1. Typical parameters represent the statistical mean values